FAIRCHILD
SEMICONDUCTOR®

December 2009

Single-Channel: 6N138M, 6N139M
Dual-Channel: HCPL2730M, HCPL2731M (Preliminary)
Low Input Current High Gain Split Darlington Optocouplers

Features

- Low current – 0.5mA
- Superior CTR-2000%
- Superior CMR-10kV/µs
- CTR guaranteed 0–70°C
- U.L. recognized (File # E90700, Vol. 2)
- VDE recognition (pending)
  – Ordering option V, e.g., 6N138VM
- Dual Channel – HCPL2730M, HCPL2731M (coming soon)

Applications

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver

Description

The 6N138M/9M and HCPL2730M/31M optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

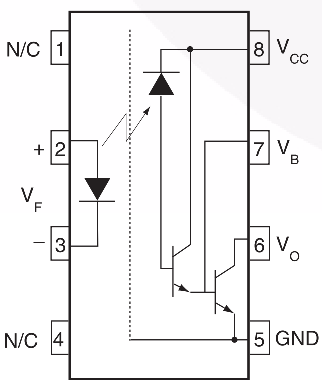
The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL2730M/HCPL2731M, an integrated emitter-base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/µs.

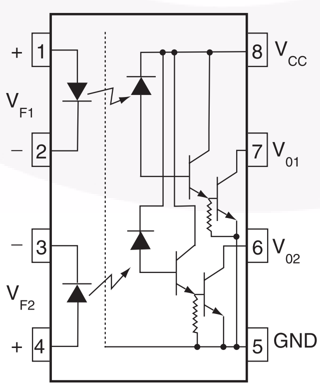
Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/HC/HCPL0700.html
- www.fairchildsemi.com/pf/HC/HCPL0730.html
- www.fairchildsemi.com/pf/HC/HCPL0731.html

Schematic

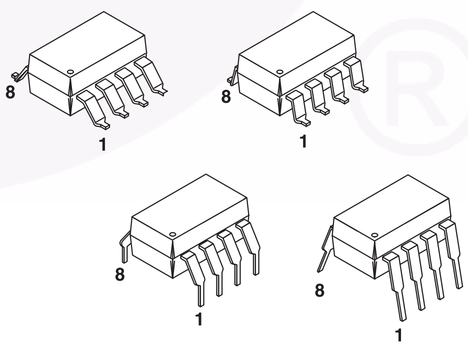


6N138M / 6N139M



HCPL2730M / HCPL2731M

Package Outlines



Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Value	Units
T_{STG}	Storage Temperature		-40 to +125	°C
T_{OPR}	Operating Temperature		-40 to +100	°C
T_{SOL}	Lead Solder Temperature (Wave solder only. See recommended reflow profile graph on page 13 for SMD mounting)		260 for 10 sec	°C
EMITTER				
I_F (avg)	DC/Average Forward Input Current	Each Channel	20	mA
I_F (pk)	Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel	40	mA
I_F (trans)	Peak Transient Input Current – (≤1µs P.W., 300 pps)		1.0	A
V_R	Reverse Input Voltage	Each Channel	5	V
P_D	Input Power Dissipation(1)	Each Channel	35	mW
DETECTOR				
I_O (avg)	Average Output Current	Each Channel	60	mA
V_{ER}	Emitter-Base Reverse Voltage	6N138M and 6N139M	0.5	V
V_{CC}, V_O	Supply Voltage, Output Voltage	6N138M and HCPL2730M	-0.5 to 7	V
		6N139M and HCPL2731M	-0.5 to 18	
P_O	Output Power Dissipation(1)	Each Channel	100	mW

Note:

1. No derating required for devices operated within the T_{OPR} specification (6N138 and 6N139 only). HCPL2730 and HCPL2731 derating TBD.

Electrical Characteristics

(T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0V.)

Individual Component Characteristics

Symbol	Parameter	Test Conditions		Device	Min.	Typ.	Max.	Unit
EMITTER								
V_F	Input Forward Voltage	Each channel (I_F = 1.6mA)	T_A = 25°C	All		1.30	1.7	V
							1.75	
BV_R	Input Reverse Breakdown Voltage	T_A = 25°C, I_R = 10µA		All	5.0	19		V
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	I_F = 1.6mA		All		-1.94		mV/°C
DETECTOR								
I_{OH}	Logic HIGH Output Current	I_F = 0mA, V_O = V_{CC} = 18V		6N139M		0.0036	100	µA
			Each Channel	HCPL2731M				
		I_F = 0mA, V_O = V_{CC} = 7V		6N138M		0.001	250	
			Each Channel	HCPL2730M				
I_{CCL}	Logic LOW supply	I_F = 1.6mA, V_O = Open, V_{CC} = 18V		6N138M, 6N139M		0.4	1.5	mA
		I_{F1} = I_{F2} = 1.6mA, V_{O1} = V_{O2} = Open	V_{CC} = 18V	HCPL2731M			3	
			V_{CC} = 7V	HCPL2730M				
I_{CCH}	Logic HIGH Supply	I_F = 0mA, V_O = Open, V_{CC} = 18V		6N138M, 6N139M		0.0003	10	µA
		I_{F1} = I_{F2} = 0mA, V_{O1} = V_{O2} = Open	V_{CC} = 18V	HCPL2731M			20	
			V_{CC} = 7V	HCPL2730M				

Transfer Characteristics

Symbol	Parameter	Test Conditions		Device	Min.	Typ.	Max.	Unit
COUPLED								
CTR	Current Transfer Ratio(2)(3)	I_F = 0.5mA, V_O = 0.4 V, V_{CC} = 4.5V		6N139M	400	2000		%
			Each Channel	HCPL2731M				
		I_F = 1.6mA, V_O = 0.4 V, V_{CC} = 4.5V		6N139M	500	1600		
			Each Channel	HCPL2731M				
		I_F = 1.6mA, V_O = 0.4 V, V_{CC} = 4.5V		6N138M	300	1600		
			Each Channel	HCPL2730M				
V_{OL}	Logic LOW Output Voltage(3)	I_F = 0.5mA, I_O = 2mA, V_{CC} = 4.5V		6N139M		0.05	0.4	V
		I_F = 1.6mA, I_O = 8mA, V_{CC} = 4.5V		6N139M		0.093	0.4	
			Each Channel	HCPL2731M				
		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V		6N139M		0.13	0.4	
			Each Channel	HCPL2731M				
		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		6N139M		0.18	0.4	
			Each Channel	HCPL2731M				
		I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		6N138M		0.06	0.4	
			Each Channel	HCPL2730M				

Electrical Characteristics (Continued)

(T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0V.)

Switching Characteristics (V_{CC} = 5V)

Symbol	Parameter	Test Conditions		Device	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic LOW[(3)] (Fig. 12)	R_L = 4.7kΩ, I_F = 0.5mA		6N139M			30	µs
			T_A = 25°C			2.5	25	
		R_L = 4.7kΩ, I_F = 0.5mA Each Channel		HCPL2731M			120	
			T_A = 25°C				100	
		R_L = 270Ω, I_F = 12mA		6N139M			2	
			T_A = 25°C			0.24	1	
		R_L = 270Ω, I_F = 12mA, Each Channel		HCPL2730M			3	
			T_A = 25°C	HCPL2731M			2	
		R_L = 2.2kΩ, I_F = 1.6mA		6N138M			15	
			T_A = 25°C			1	10	
		R_L = 2.2kΩ, I_F = 1.6mA, Each Channel		HCPL2731M HCPL2730M			25	
			T_A = 25°C				20	
t_{PLH}	Propagation Delay Time to Logic HIGH[(3)] (Fig. 12)	R_L = 4.7kΩ, I_F = 0.5mA		6N139M			90	µs
			Each Channel	HCPL2731M				
		R_L = 4.7kΩ, I_F = 0.5mA, T_A = 25°C		6N139M		13.6	60	
			Each Channel	HCPL2731M				
		R_L = 270Ω, I_F = 12mA		6N139M			10	
			T_A = 25°C			1.3	7	
		R_L = 270Ω, I_F = 12mA, Each Channel		HCPL2730M HCPL2731M			15	
			T_A = 25°C				10	
		R_L = 2.2kΩ, I_F = 1.6mA		6N138M			50	
			Each Channel	HCPL2730M HCPL2731M				
		R_L = 2.2kΩ, I_F = 1.6mA, T_A = 25°C		6N138M		7.3	35	
			Each Channel	HCPL2730M HCPL2731M				
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Logic HIGH[(4)] (Fig. 13)	I_F = 0mA, $\lvert V_{CM} \rvert$ = 10V_{P-P}, T_A = 25°C, R_L = 2.2kΩ		6N138M 6N139M	1,000	10,000		V/µs
			Each Channel	HCPL2730M HCPL2731M				
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Logic LOW[(4)] (Fig. 13)	(I_F = 1.6mA, $\lvert V_{CM} \rvert$ = 10V_{P-P}, R_L = 2.2kΩ) T_A = 25°C		6N138M 6N139M	1,000	10,000		V/µs
			Each Channel	HCPL2730M HCPL2731M				

Electrical Characteristics (Continued)

(T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0V.)

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Withstand Insulation Test Voltage(5)	RH ≤ 50%, T_A = 25°C, I_{I-O} ≤ 10µA, 50Hz, t = 1 min.	5000			V_{RMS}
R_{I-O}	Resistance (Input to Output)(5)	V_{I-O} = 500VDC		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)(5)(6)	f = 1MHz, V_{I-O} = 500V		1		pF
I_{I-I}	Input-Input Insulation Leakage Current(7)	RH ≤ 45%, V_{I-I} = 500VDC, t = 5s, HCPL2730M/2731 only		0.005		µA
R_{I-I}	Input-Input Resistance(7)	V_{I-I} = 500VDC, HCPL2730M/2731M only		10^{11}		Ω
C_{I-I}	Input-Input Capacitance(7)	f = 1MHz, HCPL2730M/2731M only		0.03		pF

Notes:

2. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
3. Pin 7 open. (6N138M and 6N139M only)
4. Common mode transient immunity in logic HIGH level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic HIGH state (i.e., V_O > 2.0V). Common mode transient immunity in logic LOW level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic LOW state (i.e., V_O < 0.8V).
5. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
6. For dual channel devices, C_{I-O} is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
7. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Electrical Characteristics (Continued) T_A = 25°C unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} = V_{OLX} \text{ (@ } I_L - I_2)}{I_L}$$

Where:

V_{DD1} = Input Supply Voltage
V_{DD2} = Output Supply Voltage
V_{DF} = Diode Forward Voltage
V_{OL1} = Logic "0" Voltage of Driver
V_{OH1} = Logic "1" Voltage of Driver
I_F = Diode Forward Current
V_{OLX} = Saturation Voltage of Output Transistor
I_L = Load Current Through Resistor R2
I_2 = Input Current of Output Gate

INPUT		R1 (V)	OUTPUT						
			CMOS @ 5V	CMOS @ 10V	74XX	74LXX	74SXX	74LSXX	74HXX
			R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)
CMOS @ 5V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 1 Resistor Values for Logic Interface

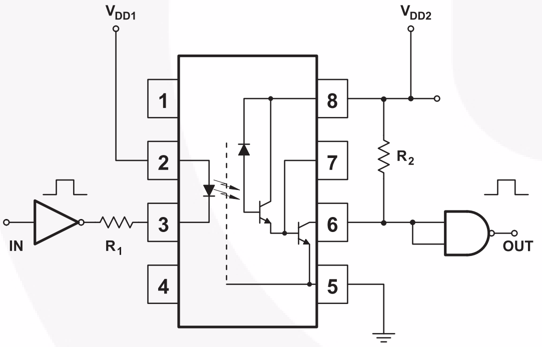


Fig. 2 Non-Inverting Logic Interface

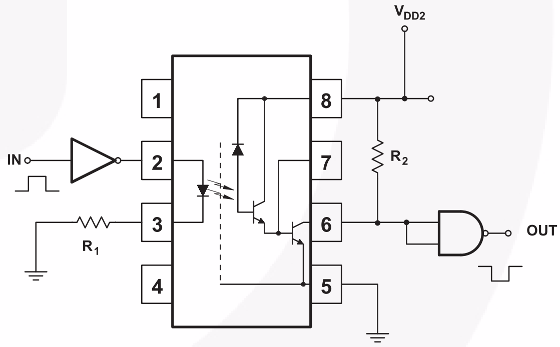


Fig. 3 Inverting Logic Interface

Typical Performance Curves

Fig. 4 LED Forward Current vs. Forward Voltage

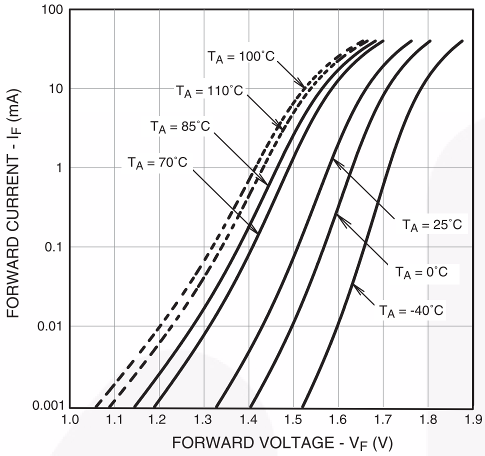


Fig. 5 LED Forward Voltage vs. Temperature

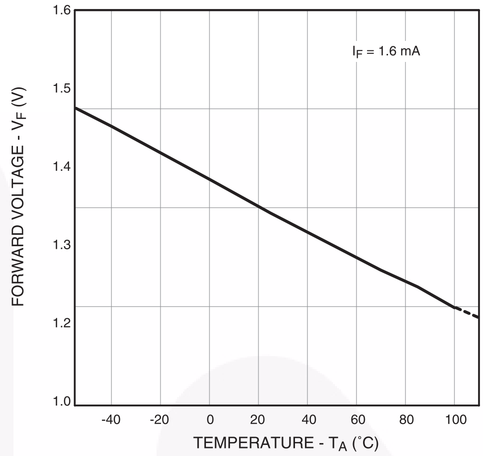


Fig. 6 Current Transfer Ratio vs. Forward Current (6N138M / 6N139M Only)

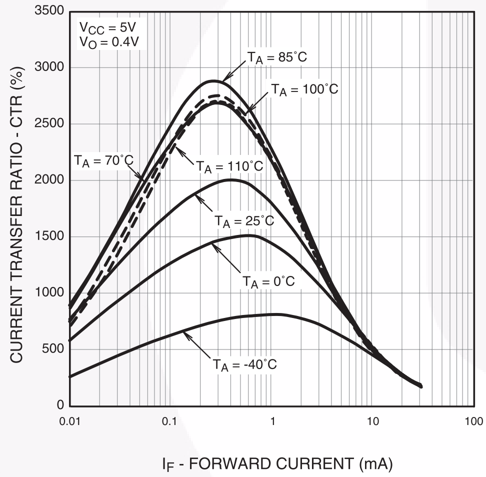


Fig. 7 Normalized Current Transfer Ratio vs. Ambient Temperature (6N138M / 6N139M Only)

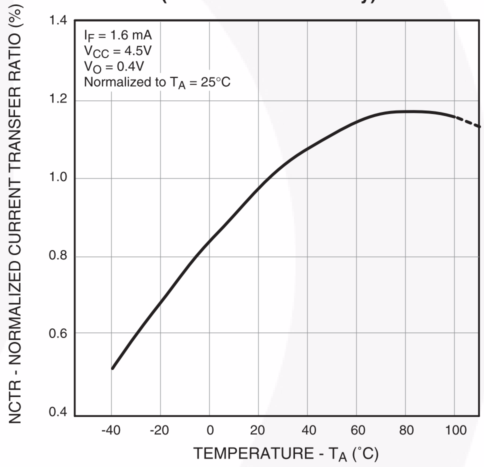


Fig. 8 Current Transfer Ratio vs. Base-Emitter Resistance (6N138M / 6N139M Only)

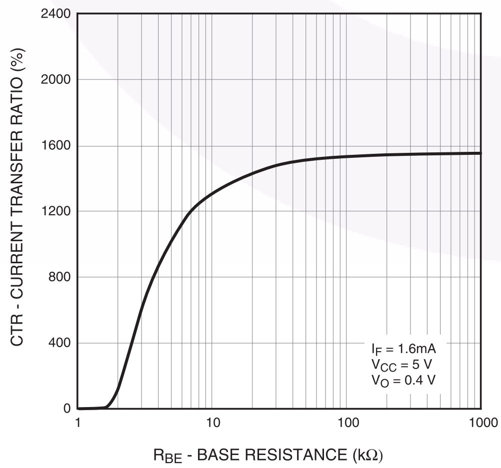
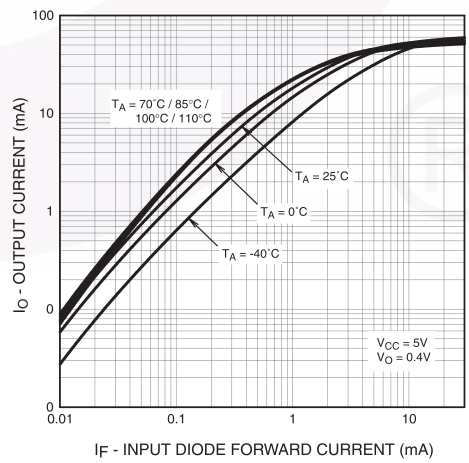


Fig. 9 Output Current vs. Input Diode Forward Current (6N138M / 6N139M Only)



Typical Performance Curves (Continued)

Fig. 10 Output Current vs Output Voltage (6N138M / 6N139M Only)

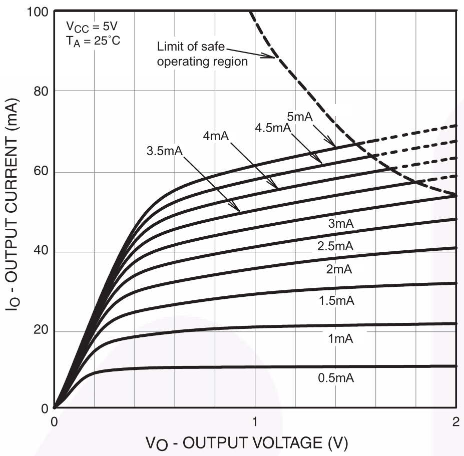


Fig. 11 Logic Low Supply Current vs. Input Diode Forward Current (6N138M / 6N139M Only)

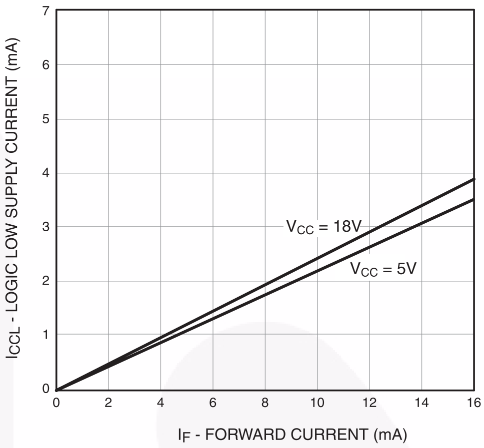
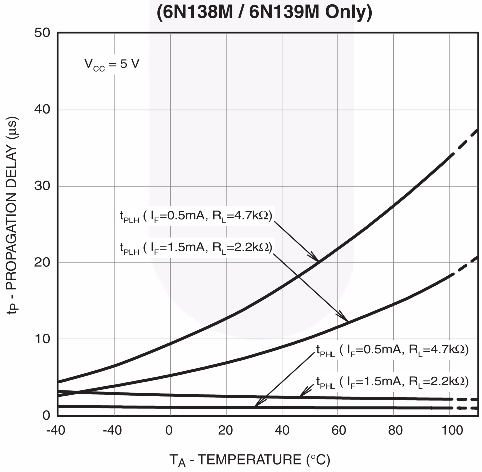


Fig. 12 Propagation Delay vs. Temperature (6N138M / 6N139M Only)



Test Circuits

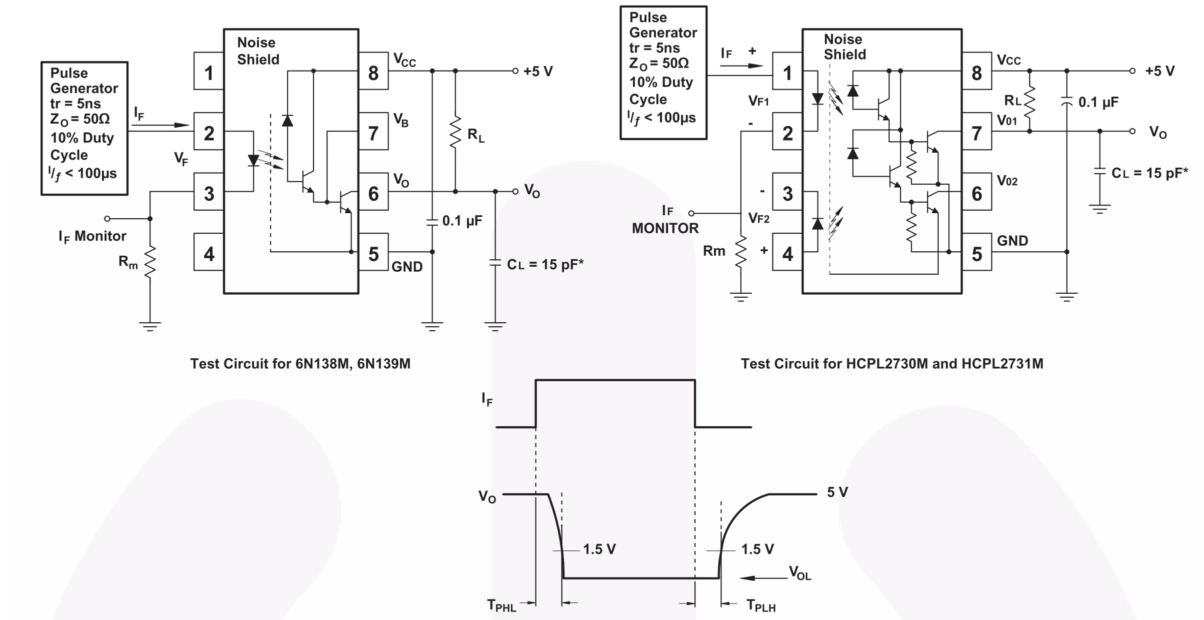


Fig. 13 Switching Time Test Circuit

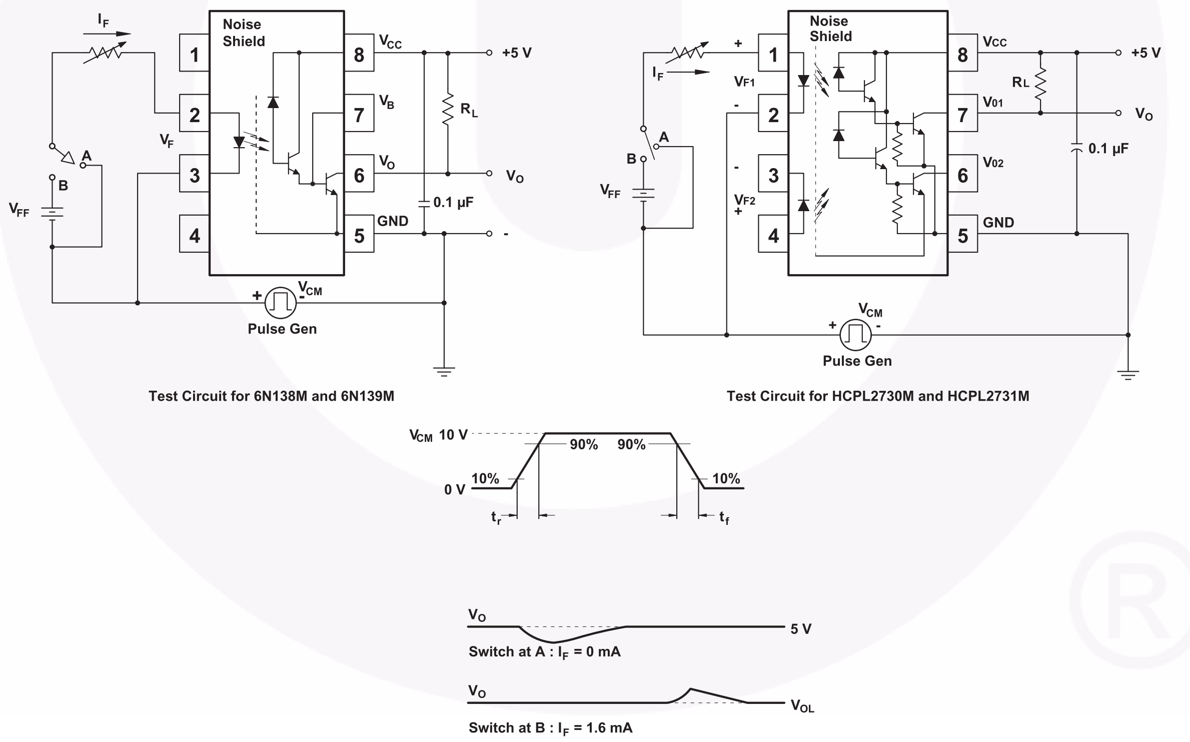
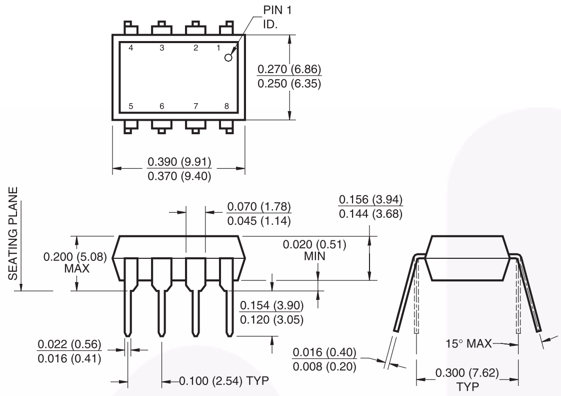


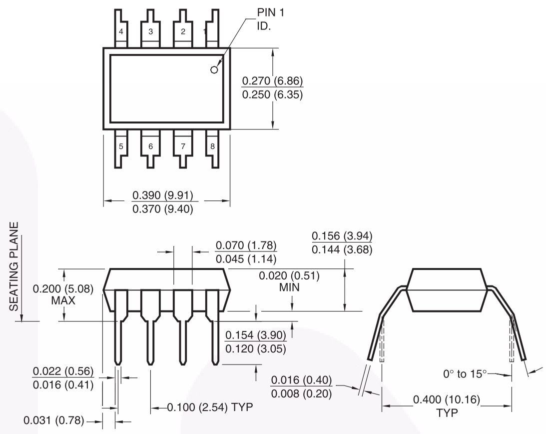
Fig. 14 Common Mode Immunity Test Circuit

Package Dimensions

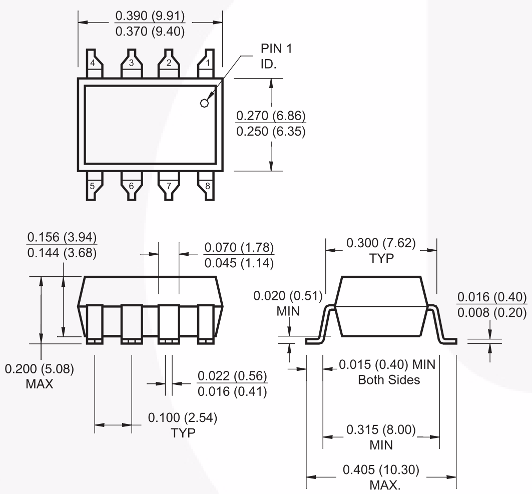
Through Hole



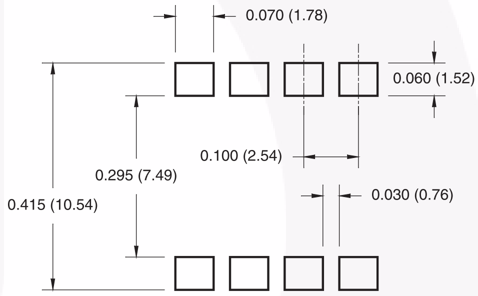
0.4" Lead Spacing (Option TV) (Pending)



Surface Mount – 0.3" Lead Spacing (Option S)



8-Pin Surface Mount DIP – Land Pattern (Option S)



Note:
All dimensions are in inches (millimeters)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

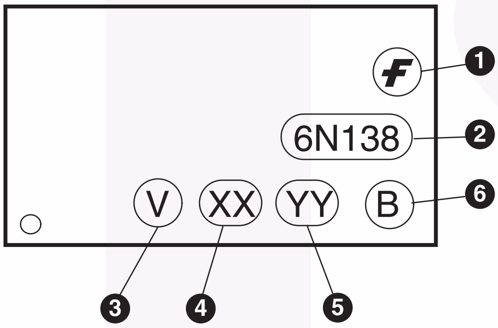
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

http://www.fairchildsemi.com/packaging/

Ordering Information

Option	Example Part Number	Description
No Suffix	6N138M	Standard Through Hole Device, 50 pcs per tube
S	6N138SM	Surface Mount Lead Bend
SD	6N138SDM	Surface Mount; Tape and reel
V	6N138VM	IEC60747-5-2 approval pending (VDE)
TV	6N138TVM	IEC60747-5-2 approval pending (VDE); 0.4" lead spacing
SV	6N138SVM	IEC60747-5-2 approval pending (VDE); surface mount
SDV	6N138SDVM	IEC60747-5-2 approval pending (VDE); surface mount; tape and reel

Marking Information



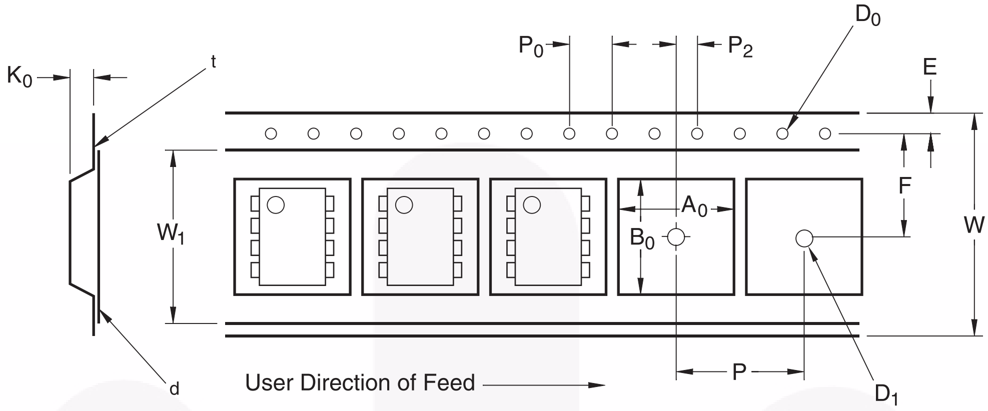
Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) (pending approval)
4	Two digit year code, e.g., '07'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

Note:

'HCPL' devices are marked only with the numerical characters (for example, HCPL2730 is marked as '2730').

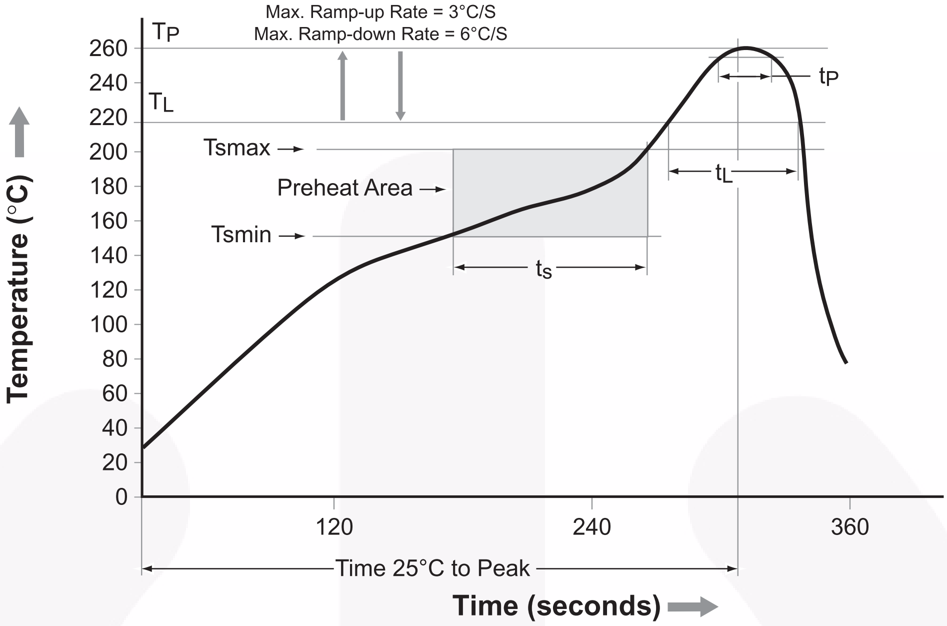
The 'M' suffix on the part number is an order identifier only. It is used to identify orders for the white package version. The 'M' does not appear on the device's top mark.

Carrier Tape Specifications (Option SD)



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ±0.20
B_0		10.30 ±0.20
K_0		4.90 ±0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second max.
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

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CTL™
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FACT Quiet Series™
FACT®
FAST®
FastvCore™
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MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
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Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
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QS™
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™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
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Definition of Terms

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