

8259A

Programmable Interrupt Controller
iAPX86 Family
MILITARY INFORMATION

8259A

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5-V supply (no clocks)
- 28-pin dual-in-line package

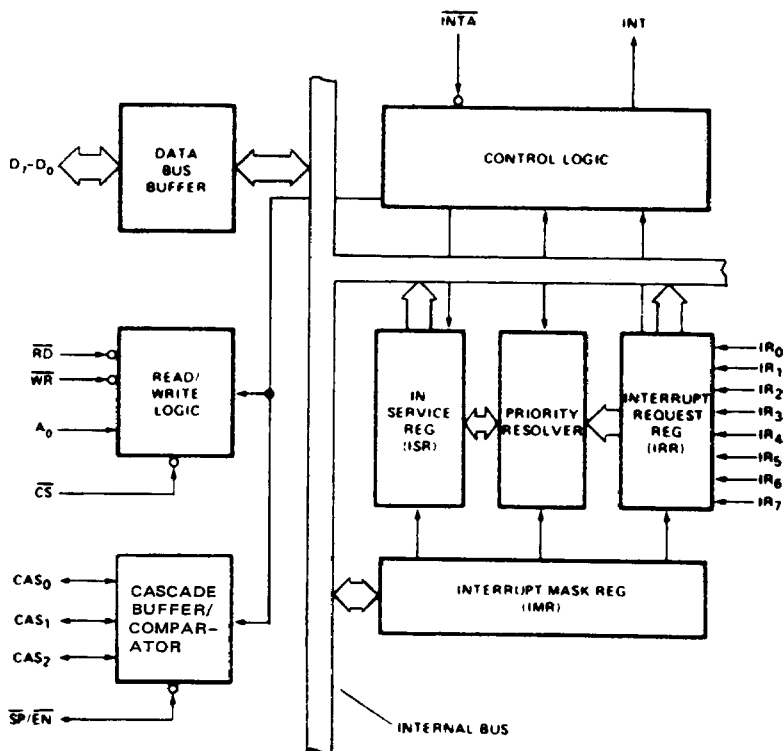
GENERAL DESCRIPTION

The 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology, and requires a single +5-V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

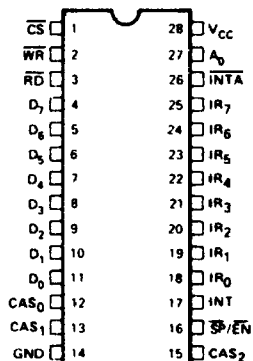
The 8259A is fully upward-compatible with the 8259. Software originally written for the 8259 will operate the 8259A in all 8259-equivalent modes.

BLOCK DIAGRAM



BD003541

CONNECTION DIAGRAM Top View



CD005642

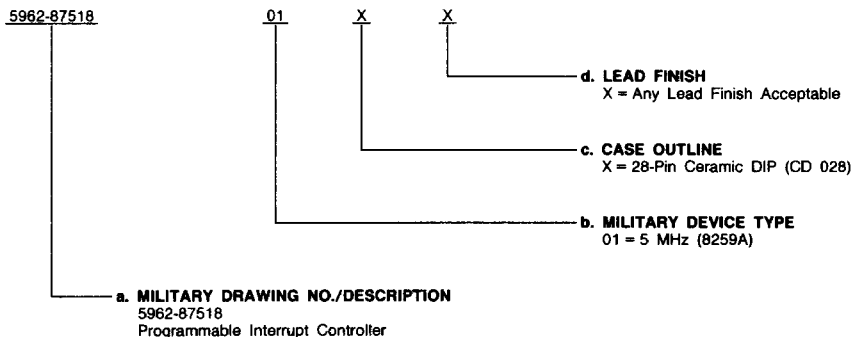
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of:

- a. Military Drawing Part Number
- b. Device Type
- c. Case Outline
- d. Lead Finish



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
5962-8751801	XX

Group A Tests

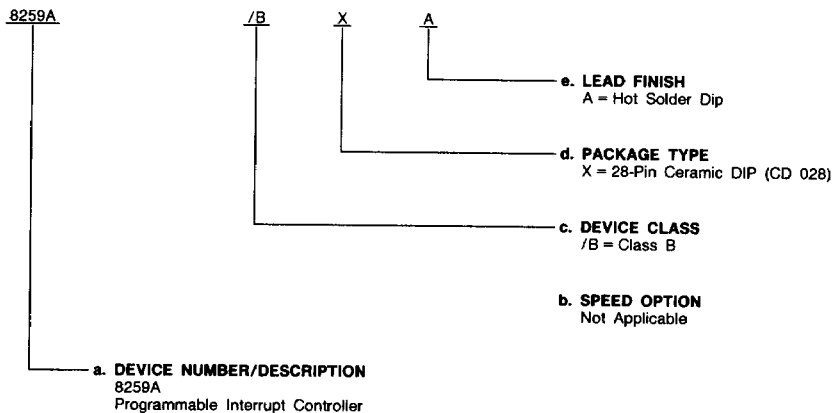
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
8259A	/BXA

Group A Tests

Group A tests consist of subgroups
1, 2, 3, 7, 8, 9 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Voltage on Any Pin
 with Respect to Ground -0.5 V to +7 V
 Power Dissipation 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices

Temperature (T_C) -55 to 125°C
 Supply Voltage (V_{CC}) 5 V $\pm$ 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-0.5*	0.8	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.3	$V_{CC} + 0.5 \text{ V}^*$	V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.2 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$		0.45	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -400 \text{ }\mu\text{A}$, $V_{CC} = 4.5 \text{ V}$		2.4	V
$V_{OH(INT)}$	Interrupt Output HIGH Voltage	$I_{OH} = -100 \text{ }\mu\text{A}$, $V_{CC} = 4.5 \text{ V}$		1.5	V
		$I_{OH} = -400 \text{ }\mu\text{A}$, $V_{CC} = 4.5 \text{ V}$		2.4	V
I_{LI}	Input Load Current	$V_{IN} = 5 \text{ V}$, $V_{IN} = 5.5 \text{ V}$ and 0 V	-10	+10	μA
I_{LOL} , I_{LOH}	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$ and 0.45 V	-10	+10	μA
I_{CC}	V_{CC} Supply Current	$V_{CC} = 5 \text{ V}$ (Note 1)		125	mA

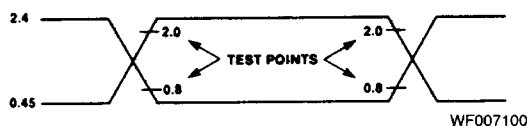
Notes: 1. I_{CC} measured in a static condition with output in worst-case state, having standard I_{OL}/I_{OH} loads applied.

CAPACITANCE (TA = 25°C, $V_{CC} = \text{GND} = 0 \text{ V}$)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
$C_{IN}^\dagger$	Input Capacitance	$f_c = 1 \text{ MHz}$		10*	pF
$C_{I/O}^\dagger$	I/O Capacitance	Unmeasured pins returned to V_{SS}		20*	pF

*Guaranteed by design; not tested.

†Not included in Group A tests.

SWITCHING TEST WAVEFORM**Input/Output**

Note: AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

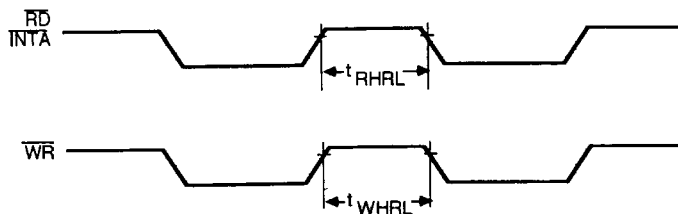
SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted).

No.	Parameter Symbol	Parameter Description	Test Conditions	8259A		Unit
				Min.	Max.	
TIMING REQUIREMENTS						
1	t _{AHRL}	A ₀ /CS Setup to RD/INTA ₁	MILITARY INFO	0		ns
2	t _{RHAX}	A ₀ /CS Hold after RD/INTA ₁		0		ns
3	t _{RLRH}	RD Pulse Width		235		ns
4	t _{AHWL}	A ₀ /CS Setup to WR ₁		0		ns
5	t _{WHAX}	A ₀ /CS Hold after WR ₁		0		ns
6	t _{WLWH}	WR Pulse Width		290		ns
7	t _{DVWH}	Data Setup to WR ₁		240	(Note 1)	ns
8	t _{WHDX}	Data Hold after WR ₁		0		ns
9	t _{LJLH}	Interrupt Request Width (LOW)		100		ns
10	t _{CVIAL}	Cascade Setup Second or Third INTA ₁ (Slave Only)		55		ns
11	t _{AHRL}	End of RD to next Command		300		ns
12	t _{WHRL}	End of WR to next Command		370		ns

TIMING RESPONSES

13	t_{RLOV}	Data Valid from $\overline{RD}/\overline{INTA}_1$	(Notes 1 and 2)		200	ns
14	t_{RHOZ}	Data Float after $\overline{RD}/\overline{INTA}_1$		10	100	ns
15	t_{JHIH}	Interrupt Output Delay			350	ns
16	t_{IALCV}	Cascade Valid from First $\overline{INTA}_1$ (Master Only)			565	ns
17	t_{RLEL}	Cascade Inactive from $\overline{RD}_1$ or $\overline{INTA}_1$			125	ns
18	t_{RHEH}	Cascade Inactive from $\overline{RD}_1$ or $\overline{INTA}_1$			150	ns
19	t_{AHDV}	Data Valid from Stable Address			200	ns
20	t_{CVDV}	Cascade Valid to Valid Data			300	ns

Notes: 1. Test Conditions: $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
 $V_{IL} = 0.45 \text{ V}$, $V_{IH} = 2.4 \text{ V}$; $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$
 $I_{OL} = 2.2 \text{ mA}$, $I_{OH} = -400 \mu\text{A}$
 2. Test Condition: $C_L = 100 \text{ pF} \pm 20 \text{ pF}$.



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Other Timing (Military)