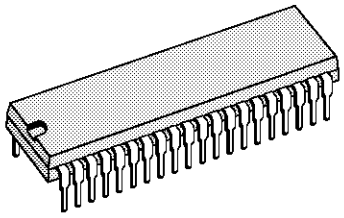
SGS-THOMSON MICROELECTRONICS

TS9347

SINGLE CHIP SEMI–GRAPHIC DISPLAY PROCESSOR

- SINGLE CHIP LOW-COST CRT CONTROLLER
- UP TO 60 Hz SCREEN REFRESH RATE
- 32 KBYTE DEDICATED MEMORY ADDRESSING SPACE
- 2 SCREEN FORMATS :
  25 ROWS OF 40 CHARACTERS
  25 ROWS OF 80 CHARACTERS
- ON-CHIP 154 ALPHANUMERIC AND 128 SEMIGRAPHIC CHARACTER GENERATOR
- EASY EXTENSION OF USER DEFINED ALPHANUMERIC OR SEMI-GRAPHIC SETS (>1K characters)
- 40 CHARACTERS/ROW ATTRIBUTES : FOREGROUND AND BACKGROUND COLOR, DOUBLE HEIGHT, DOUBLE WIDTH, BLINKING, CONCEAL, INSERT
- 80 CHARACTERS/ROW ATTRIBUTES : UNDERLINING, BLINKING, REVERSE, COLOR SELECT
- PROGRAMMABLE ROLL-UP, ROLL-DOWN, UPPER OR LOWER SERVICE ROW
- ON-CHIP R, G, B SHIFT REGISTERS
- ANALOG COMPOSITE LUMINANCE SIGNAL OUTPUT
- VERSATILE I/O CONFIGURATION : VIDEO AND SYNC OR GENERAL PURPOSE I/O PORTS
- ADDRESS/DATA MULTIPLEXED BUS DIRECTLY COMPATIBLE WITH STANDARD MICROCOMPUTERS SUCH A 6801, 6301, 8048, 8051



P
DIP40
(Plastic Package)

DESCRIPTION

A complete display control unit may be implemented with TS9347 and a single standard memory package. This new advanced CRT controller drastically reduces IC cost and PCB area for low-end color or monochrome terminal.

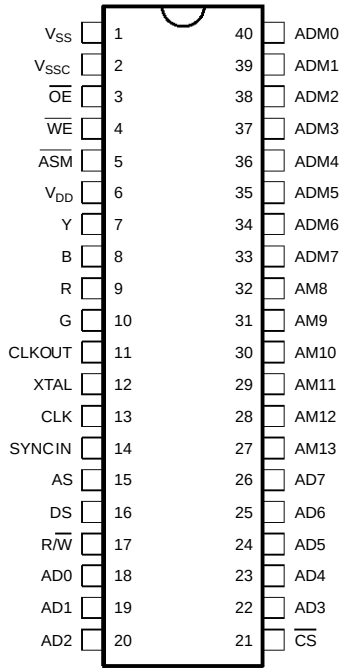
ORDERING INFORMATION

Part Number	Package	Pin Configuration
TS9347CP/1R00	DIP40	1R00
TS9347CP/2R00	DIP40	2R00

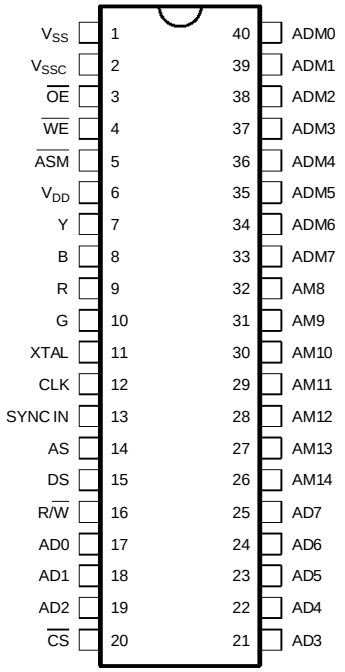
9347-01.TBL

PIN CONNECTIONS

DIP40
TS9347CP/1R00



DIP40
TS9347CP/2R00



9347-01.EPS - 9347-02.EPS

PIN DESCRIPTION (All the input/output pins, XTAL and Y excepted, are TTL compatible)

Name	Pin Type	Function	Description
MICROPROCESSOR INTERFACE			
AD (0:7)	I/O	Multiplexed Address/Data Bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	Address Strobe	The falling egde of this control signal latches the address on the AD (0:7) lines, the state of the Data Strobe (DS) and Chip Select (CS) into the chip.
DS	I	Data Strobe	- When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle (R/W = 1). In write cycle, data present on AD (0:7) lines are strobed by R/W low (see timing diagram 2). - When this input is strobed low by AS, R/W gives the direction of data transfer on AD (0:7) bus. DS high strobes the data to be written during a write cycle (R/W = 0) or enables the output buffers during a read cycle (R/W = 1) (see timing diagram 1).
R/W	I	Read/Write	This input determines whether the internal registers get written or read. A write is active low (”0”).
CS	I	Chip Select	The TS9347 is selected when this input is strobed low by AS.
MEMORY INTERFACE			
ADM (0:7)	I/O	Multiplexed Address/Data Bus	Lower 8 bits of memory address appear on the bus when ASM is high. It the becomes the data bus when ASM is low.
AM (8:14)	O	Memory Address/Data Bus	Theses 7 pins provide the high order bits of the memory address.
OE	O	Output Enable	When low, this output selects the memory data output buffers.

9347-02.TBL

PIN DESCRIPTION (continued)

Name	Pin Type	Function	Description
MEMORY INTERFACE (continued)			
$\overline{WE}$	O	Write Enable	This output determines whether the memory gets read or written. A write is active low (”0”).
$\overline{ASM}$	O	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.
VIDEO INTERFACE			
R	O	Red/ Composite Sync	- When TGS_5 = 0, this output delivers the Red component of the video signal. It is low during the H and V blanking intervals. - When TGS_5 = 1, this output delivers the composite synchronization signal.
G	O	Gree/Insert/Port1	- When TGS_4 = TGS_5 = 0, this output delivers the Green component of the video signal. It is low during the V and H blanking intervals. - When TGS_4 = 1, this output delivers the insert attribute. It allows to insert the video signals in another external video for captionning purposes for example. It can also be used as a general purpose attribute or color. - When TGS_5 = 1 and TGS4 = 0, this pin is a general purpose output port. Its state is programmed by the value of PAT2.
B	O	Blue/Port2	- When TGS_5 = 0, this output delivers the Blue component of the video signal. It is low during the V and H blanking intervals. - When TGS_5 = 1, this pin is a general purpose output port programmed by the value of PAT7.
Y	O	Composite Luminance	This analog output delivers the composite luminance signal with 8 different grey levels plus the synchronization level.
Sync	I	Sync. Input/ Input Port	- When TGS_3 = 1, this input allows to vertically and, if TGS_2, is set, horizontally synchronize the TS9347 on an external signal. - When TGS_2 = TGS_3 = 0, the logic state of this input may be read by the microprocessor, and acts as a general purpose input port. - This input must be grounded if not used.
OTHERS PINS			
CLK XTAL	I/O	Crystal/Clock Input Crystal Output	These pins allow to connect a crystal to generate the input frequency from 12 to 15MHz. If an external signal is used, it must be applied on CLK input, XTAL is left unconnected.
CLK OUT	O	Clock Output	When internal oscillator is used, this pin provides a TTL compatible oscillator output for general operation.
V_{SS}	S	Power Supply	Ground
V_{DD}	S	Power Supply	+5V
V_{SSC} V_{DDC}	S	Power Supply Power Supply	These pins provide separate 0V and 5V power supply for the Y analog converter, allowing easier noise reduction.

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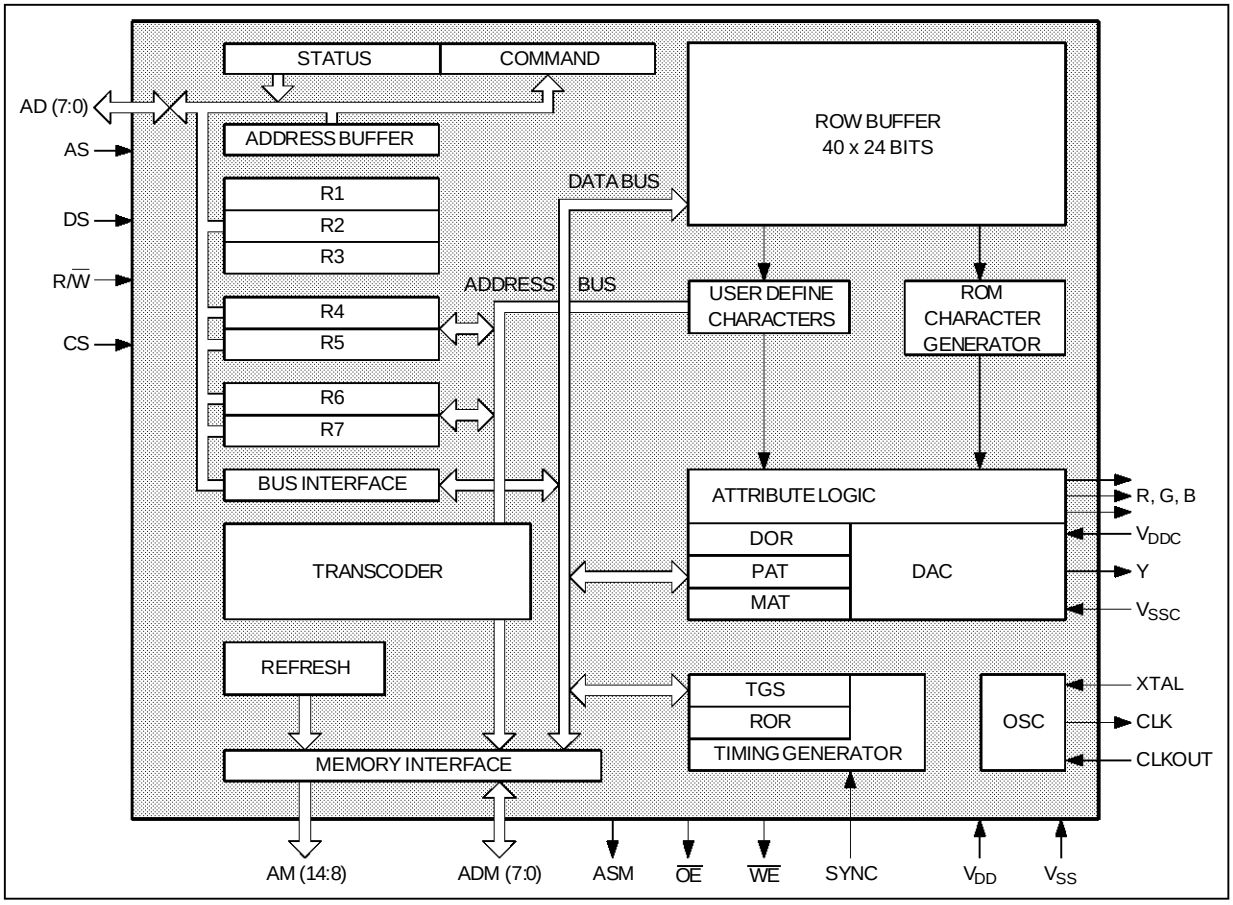
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	0.3, 7.0	V
V_{IN}*	Input Voltage	0.3, 7.0	V
T_A	Operating Temperature Range	0, +70	°C
T_{stg}	Storage Temperature Range	-55, +150	°C
P_{Dm}	Max. Power Dissipation	0.75	W

9347-04.TBL

* With respect to V_{SS}.

** Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operations (sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL OPERATING CHARATERISTICS

V_{CC} = 5.0V ±5%, V_{SS} = 0, T_{amb} = 0 to 70°C (unless otherwise specified)

Symbol	Parameter	Mln.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{IH}	Input High Voltage CLK (external CLK) Other Inputs	2.2 2	- -	V_{CC} V_{CC}	V -
I_{IN}	Input Leakage Current (execpt CLK)	-	-	10	µA
V_{OH}	Output HIgh Voltage (I_{load} = 500µA)	2.4	-	-	V
V_{OL}	Output Low Voltage I_{load} = 4mA : AD (0:7), ADM (0:7) I_{load} = 1 mA : Other Outputs Except Y	-	-	0.4	V
P_D	Power Dissipation	-	350	500	mW
C_{IN}	Input Capacitance	-	-	15	pF
I_{TSI}	Three State (off state) Input Current	-	-	10	µA
t_{start}	Crystal Oscillator Start Time	-	-	1	ms

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Figure 1 : On Chip Oscillator

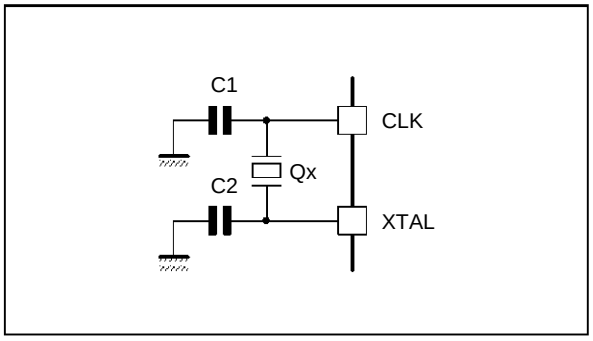

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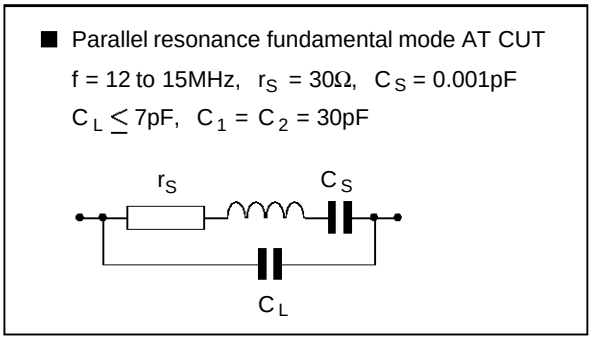
Figure 2 : Typical Crystal Parameters



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MEMORY INTERFACE

MEMORY INTERFACE CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_{amb} = 0 to +70°C)
Clock : Duty Cycle 40 to 60% ; t_r, t_f < 5ns, V_{IH} = 2.2V
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V, V_{OL} = 0.4V and V_{OH} = 2.4V

Ident. Number	Symbol	Parameter	F_{IN} = 12MHz		F = 1/T		Unit
			Min.	Max.	MIn.	Max.	
1	t_{ELEL}	Memory Cycle Time	500		6T		ns
2	t_D	Output Delay Time from CLK Rising Edge ($\overline{ASM}$, $\overline{OE}$, $\overline{WE}$)	-	60	-	60	ns
3	t_{EHEL}	ASM High Pulse Width	120	-	2T -33	-	ns
4	t_{ELDV}	Memory Access Time from $\overline{ASM}$ Low	-	250	-	4T -43	ns
5	t_{DA}	Output Delay Time from CLK Rising Edge ADM (0:7), AM (8:14)	-	80	-	80	ns
6	t_{AVEL}	Address SEtup Time to $\overline{ASM}$	30	-	T -49	-	ns
7	t_{ELAX}	Address HOld Time from $\overline{ASM}$	55	-	T -21	-	ns
8	t_{CLAZ}	Address off Time	-	80	-	80	ns
9	t_{GHDX}	Memory Hold Time	10	-	10	-	ns
10	t_{OZ}	Data off Time from $\overline{OE}$	-	60	-	T -19	ns
11	t_{GLDV}	Memory $\overline{OE}$ Access Time	-	150	-	2T -16	ns
12	t_{QVWL}	Data Setup Time (write cycle)	30	-	T -49	-	ns
13	t_{WHQX}	Data Hold Time (write cycle)	30	-	T -49	-	ns
14	t_{WLWH}	$\overline{WE}$ Pulse Width	110	-	2T -48	-	ns

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Figure 3 : Test Load

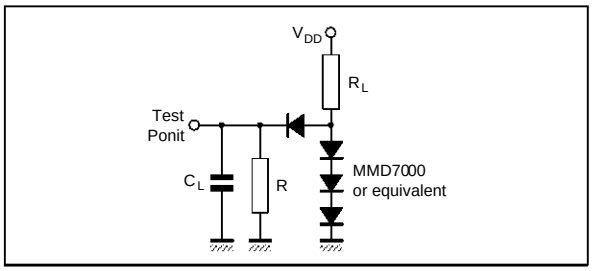

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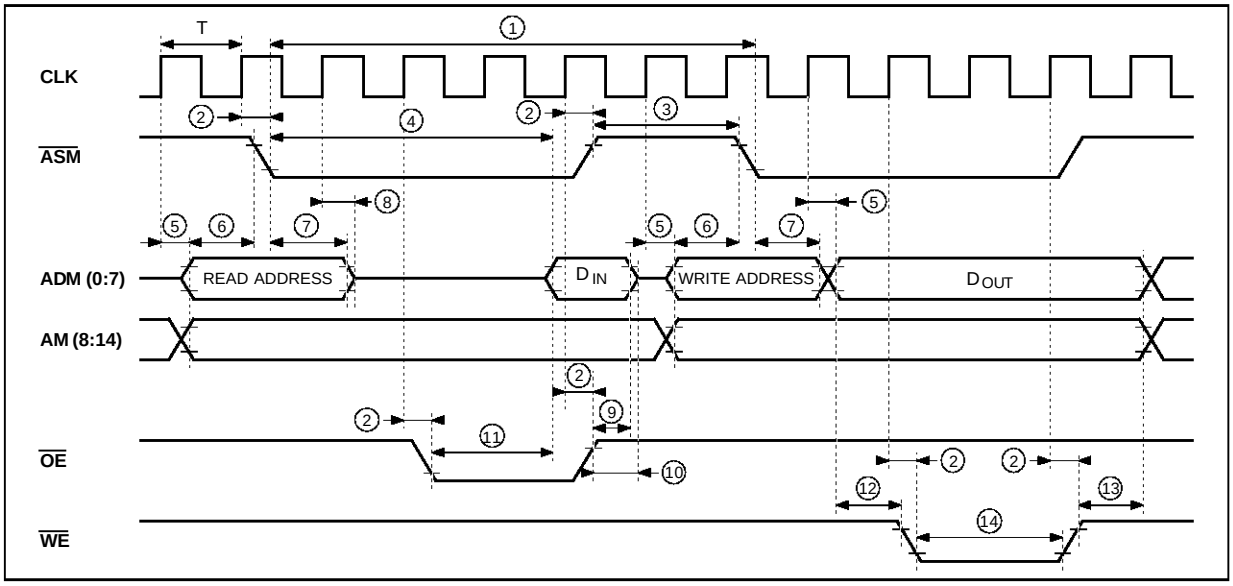
Table 1

Symbol	ADM (0, 7) AD (0, 7)	Other Outputs Except Y
C	100pF	50pF
R_L	1kΩ	3.3kΩ
R	4.7kΩ	4.7kΩ

9347-07.TBL

Figure 4 : Memory Interface Timing Diagram



9347-08.EPS

MICROPROCESSOR INTERFACE

TS9347 is MOTEL compatible. It automatically selects the processor type by using AS input to latch to state of the DS input.

No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

TS9347	6801	INTEL Family
	Timing 1	Timing 2
AS	AS	ALE
DS	DS, E, ∅2	$\overline{RD}$
R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$

9347-08.TBL

MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS (AD (0:7), AS, DS, R/$\overline{W}$, $\overline{CS}$)

V_{CC} = 5.0 ±5%, T_A = 0 to 70°C, C_L = 100pF on AD (0:7)

Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V on All Inputs ; V_{OL} = 0.4V and V_{OH} = 2.4V on All Outputs.

Ident. Number	Symbol	Parameter	Mln.	Typ.	Max.	Unit
1	t_{CYC}	Cycle Time	400	-	-	ns
2	t_{ASD}	DS Low to AS High (timing 1) DS High or R/W High to AS High (timing 2)	26	-	-	ns
3	t_{ASED}	AS Low to DS High (timing 1) AS High or DS Low or R/W Low (timing 2)	30	-	-	ns
4	t_{PWEH}	Write Pulse Width	200	-	-	ns
5	t_{PWASH}	AS Pulse Width	76	-	-	ns
6	t_{RWS}	R/$\overline{W}$ to DS Setup Time (timing 1)	100	-	-	ns
7	t_{RWH}	R/$\overline{W}$ to DS Hold Time (timing 1)	10	-	-	ns
8	t_{ASL}	Address and $\overline{CS}$ Setup Time	20	-	-	ns
9	t_{ASH}	Address and $\overline{CS}$ Hold Time	20	-	-	ns
10	t_{DSW}	Data Setup Time (write cycle)	100	-	-	ns
11	t_{DHW}	Data Hold Time (write cycle)	10	-	-	ns
12	t_{DDR}	Data Access Time from DS (read cycle)	-	-	150	ns
13	t_{DHR}	DS Inactive to High Impedance State Time (read cycle)	10	-	63	ns
14	t_{ACC}	Address to Data Valid Access Time	-	-	300	ns

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Figure 5 : Microprocessor Interface Timing Diagram 1 (6801)

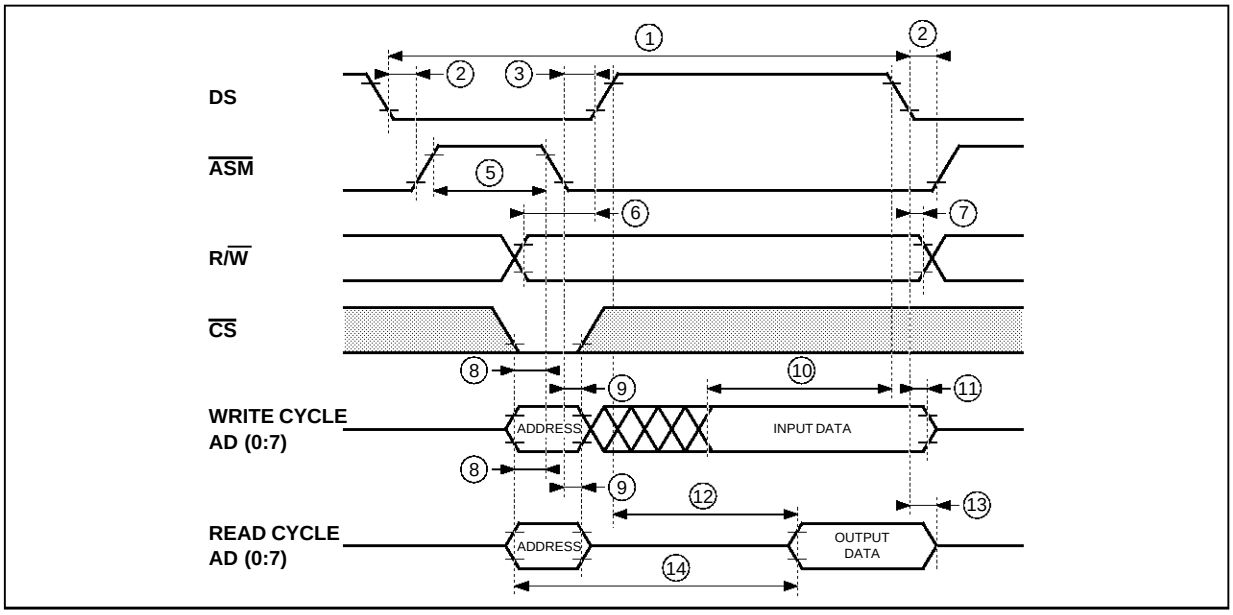

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Figure 6 : Microprocessor Interface Timing Diagram 2 (INTEL type) - READ CYCLE

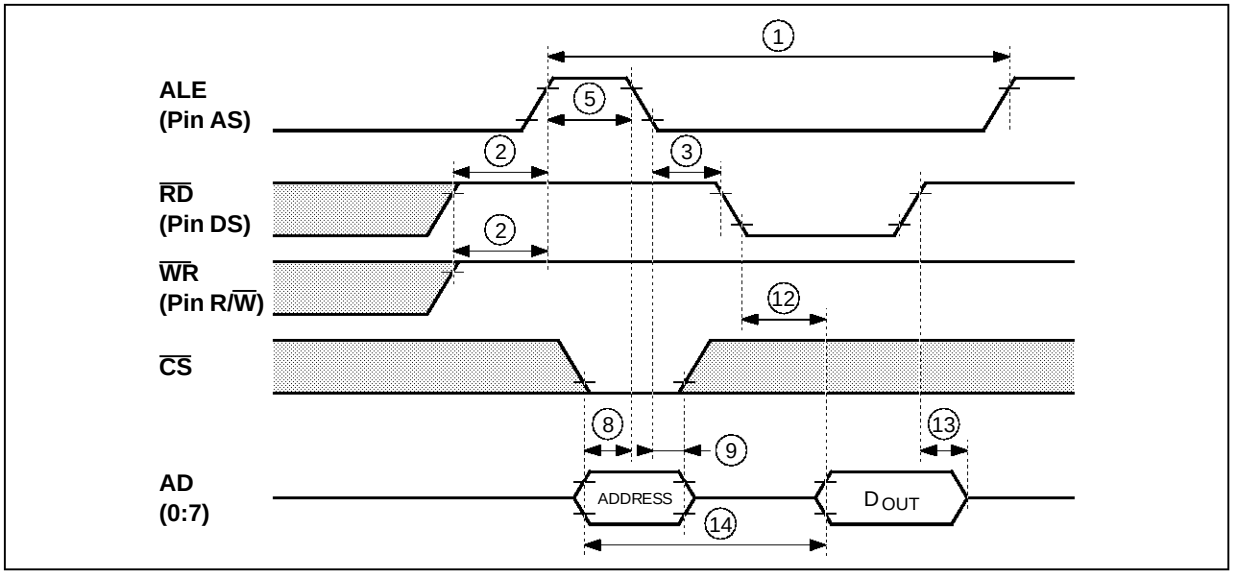
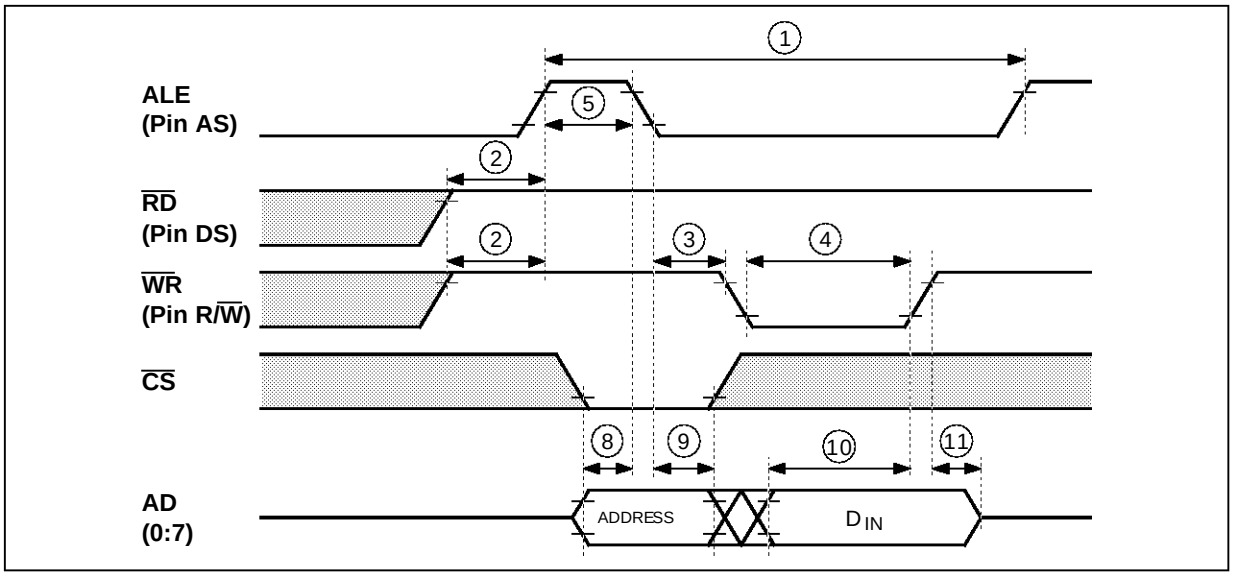


Figure 7 : Microprocessor Interface Timing Diagram 2 (INTEL type) - WRITE CYCLE



VIDEO INTERFACE R. G. B. I.

V_{CC} = 5.0V ±5%, T_{amb} = 0 to +70°C, CLK Duty Cycle 50%, C_L = 50pF
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2.2V on CLK Inputs
V_{OL} = 0.4V and V_{OH} = 2.4V on All Outputs.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_D	Output Delay from CLK Edge	-	-	60	ns

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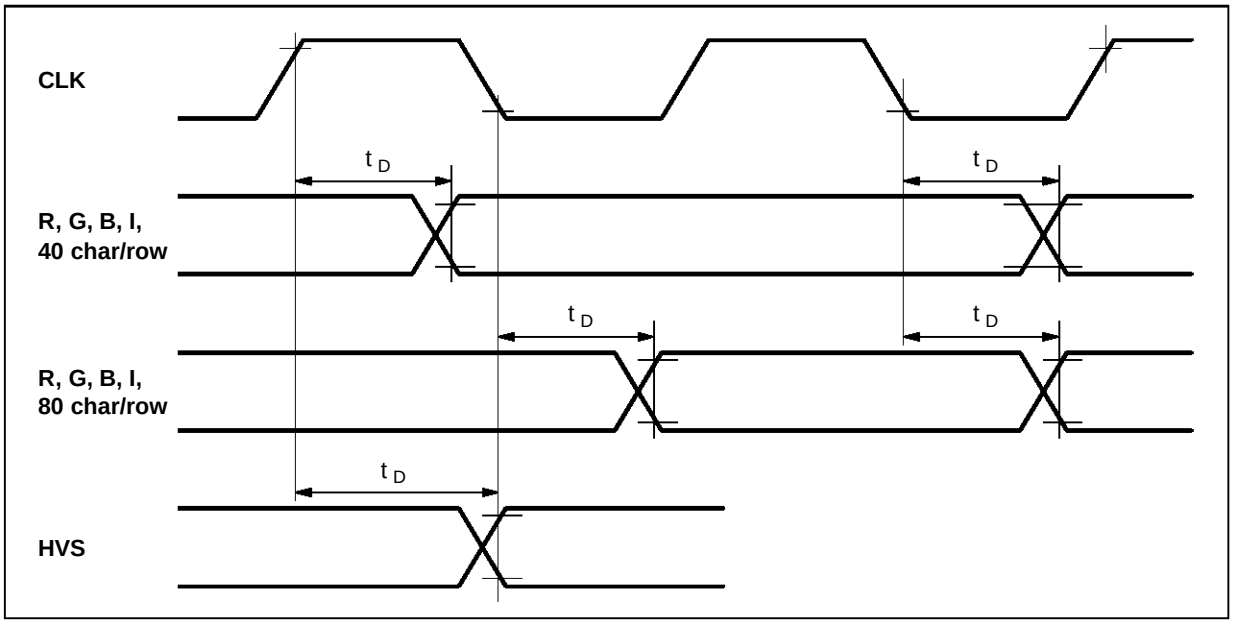
Figure 8



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INPUT CLK

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PWCH}	CLK High Pulse Width	25	-	-	ns
t_{PWCL}	CLK Low Pulse Width	25	-	-	ns
t_{rc}, t_{fc}	CLK Rise and Fall Time	-	-	10	ns
t_{WCOH}	CLKOUT High Pulse Width	20	-	-	ns
t_{WCOL}	CLKOUT Low Pulse Width	20	-	-	ns
t_{rco}, t_{fco}	CLKOUT Rise and Fall Time	-	-	20	ns

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Figure 9 : Case of External CLK Generation

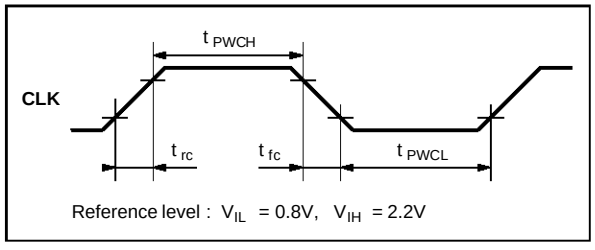

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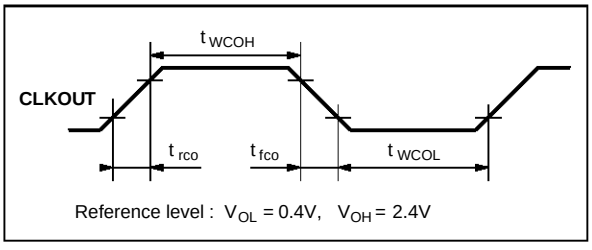
Figure 10 : Case of Internal Oscillator (f_{IN} = 12MHz)



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Y OUTPUT : Composite Luminance.

REFERENCE LEVEL

$V_{DDC} = V_{DD} = 5V$, $V_{SSC} = V_{SS} = 0V$

G	R	B	Signal	Level (V)
0	0	0	SYNC	0.06
0	0	0	BLACK	0.50
0	0	1	BLUE	0.80
0	1	0	RED	0.92
0	1	1	MAGENTA	1.03
1	0	0	GREEN	1.15
1	0	1	CYAN	1.26
1	1	0	YELLOW	1.38
1	1	1	WHITE	1.50

9347-12.TBL

ELECTRICAL SPECIFICATION

Over Full Temperature Range : $V_{DDC} = V_{DD} = 5V$ (see note 1)
$V_{SSC} = V_{SS} = 0V$, $C_L = 20pF$, $R_L > 100k\Omega$ to V_{SS} or V_{DD}

Parameter	Min.	Typ.	Max.	Unit
Monotonicity		Guaranteed		
Output Level Dispersion	-	10	50	mV
Propagation Delay (clock edge to 50% output)	-	-	60	ns
Rise and Fall Time (10 - 90%)	-	-	30	ns
Output Static Impedance	-	-	600	Ω

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Note : 1. The DAC is a 9 output potentiometric divider : therefore, each voltage variation on V_{DDC} is repercuted on the output with the same relative value with respect to V_{SSC}.

Figure 11 : Typical Application

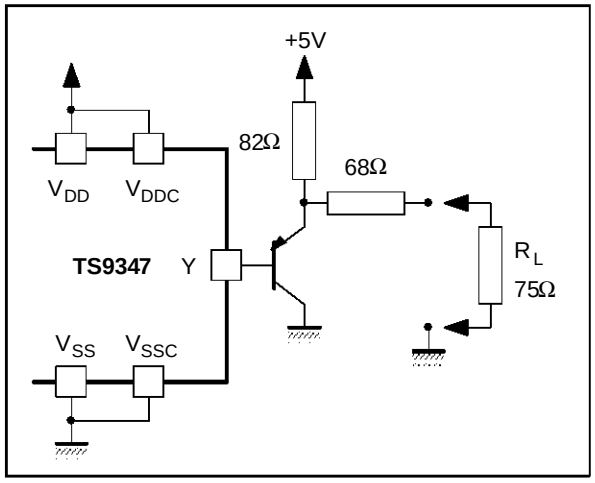

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Figure 12 : Test Condition

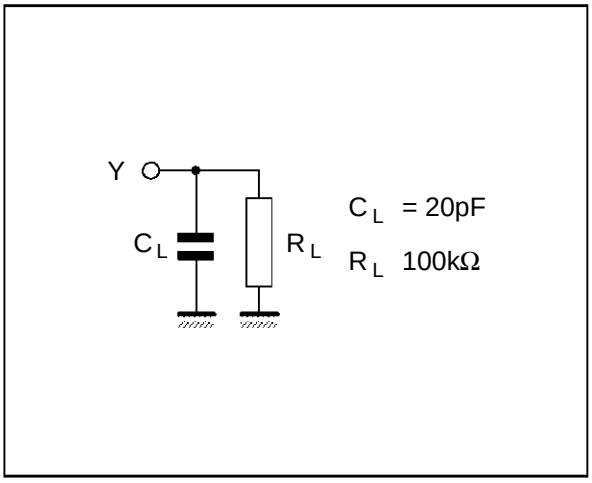

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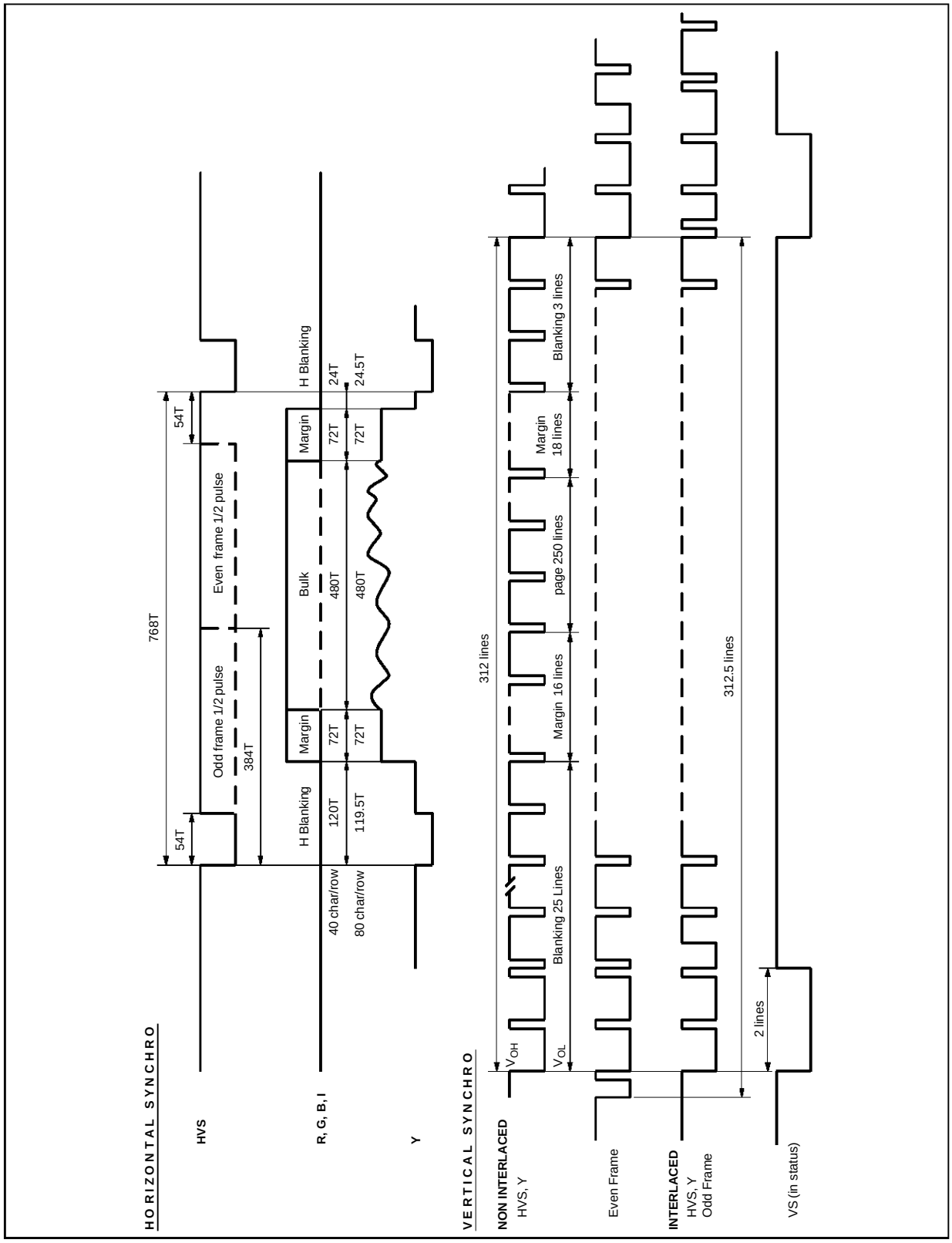
Figure 13 : Vertical and Horizontal Synchronization Outputs ($T \frac{1}{f_{CLK}}$)



FUNCTIONAL DESCRIPTION

The TS9347 is a low cost, semigraphic, CRT controller.

The TS9347 displays up to 25 rows of 40 characters or 25 rows of 80 characters, including either an upper or lower service row.

The on-chip character generator provides a standard, 5 x 7, character set and standard semigraphic sets.

More user definable (8x10) alphanumeric or semigraphic sets may be mapped in the 32 K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

Microprocessor Interface

The TS9347 provides an 8-bit, address/data multiplexed, microprocessor interface.

It is directly compatible with popular (6801, 8048, 8051, 8085....) microprocessors.

Registers

The microprocessor directly accesses 8 registers :
- R0 : Command/status register
- R1 : R2, R3 : Data registers
- R4, R5, R6, R7 : Each of these register pairs points into the private memory.

Through these registers, the microprocessor indirectly accesses the private memory and 5 more registers :
- ROR, DOR : Base address of displayed page memory and of user external character generators.
- PAT, MAT, TGS : Used to select the I/O configuration, the page attributes and format, and to program the timing generator options.

Private Memory

The user may partition the 32 K x 8 private memory addressing space between :
- pages of character codes (2 K x 8 or 3 K x 8),
- external character generators,
- general purpose user area.

Many types of memory components are suitable :
- ROM, DRAM or SRAM,
- 2 K x 8, 8 K x 8, 16 K x 4, 32 K x 8 organization,
- Modest 400ns cycle time and 240ns access time is required.

40 Characters per Row : Character Code Formats and Attributes

Once the 40 characters per row format has been selected, one character code format out of two must be chosen :
- 24-bit format
  All the attributes are provided in parallel.
- 16-bit format :
  Some parallel attributes, others are latched.

The 16-bit fixed format is compatible with EF9345 CRT controller.
Character attributes provided :
- Back ground and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- 11 x 100 user definable character generator in memory.

80 Characters per Row Format : Character Code Format and Attributes

Two character code formats are provided :
- Long (12 bits) with 4 parallel attributes :
  Blinking, Underlining, Reverse, Color select
- Short (8 bits) : no attributes.

Timing Generator

The whole timing is derived from a 12 to 15MHz on chip oscillator.

The RGB outputs are shifted at 8 to 10MHz for the 40 character/row format and at 12 to 15MHz for the 80 character/row.

The timing generator allows different display modes :
- Interlaced or not
- Master or slave synchronization.

Video Output

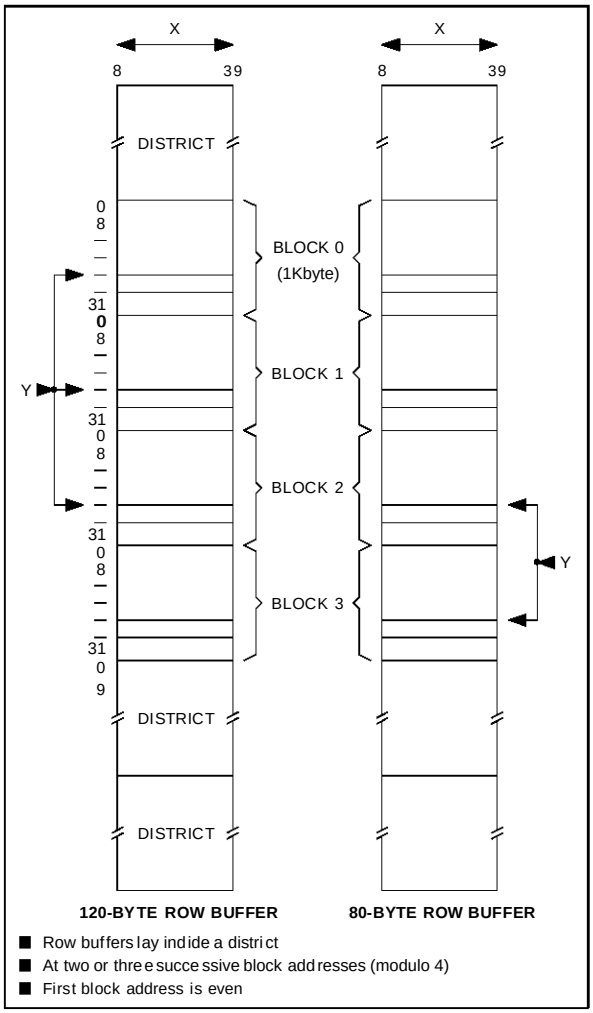
The video output is always available as a composite luminance signal on the analog output Y ; the logic R, V, B, Syncout and Insert components may be selected on the RGB output pins.

MEMORY ORGANIZATION

Logical and Physical Addressing

The physical 32 Kbyte addressing space is logically partitioned by the TS9347 into 40-byte buffers (Figure 15). More precisely, a logical address is given by an X, Y, Z triplet where :
- X = (0 to 39) points to a byte inside a buffer,
- Y = (0,8 to 31) points to a buffer a 1 Kbyte block,
- Z = (0 to 31) points to a block.

Figure 14 : Memory Row Buffer



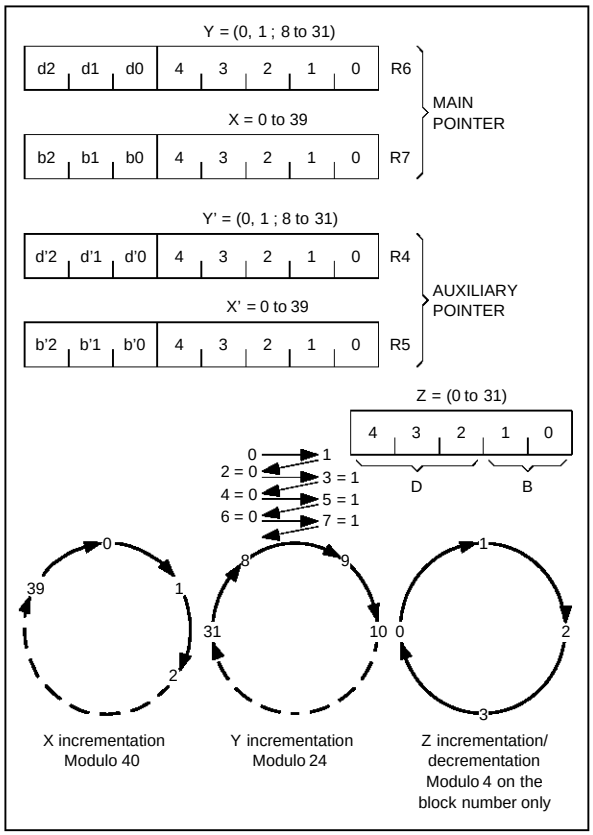
Pointers

Each X, Y, and Z component of a logical address is binary encoded and packed in two 8-bit registers. Such a register pair is a pointer (Figure 15). TS9347 contains two pointers :
- R6, R7 : main pointer
- R4, R5 : auxiliary pointer.

Both pointers have the same format. R7 (resp. R5) holds the X component and the two LSB's of the Z component. R6 (resp R4) holds the Y component and the three MSB's of the Z component. This package induce a partitionning of Z in 8 districts of 4 blocks each.

Logical to physical translation is performed on chip following Figure 16 scheme.

Figure 15 : Pointer Auto Incrementation



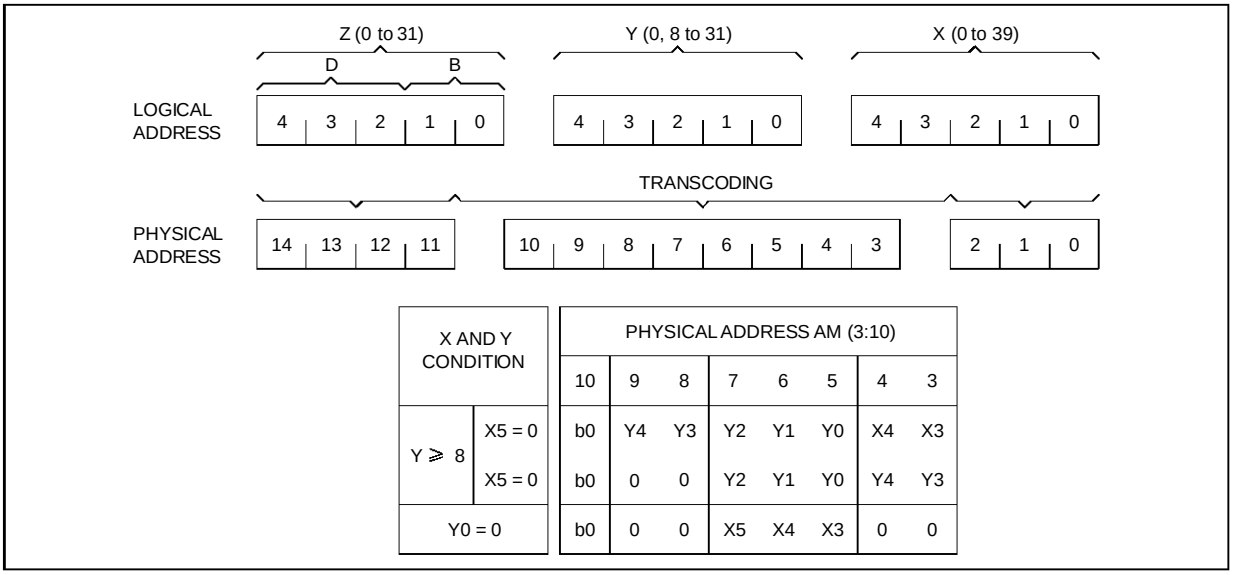
Data Structures in Memory

A page is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row buffer (Figure 14). The buffers belonging to a row buffer must meet the following requirements :
- they have the same Y address,
- they have the same district number,
- they lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.

A Page is a set of successive row buffers :
- with the same format,
- with the same district number,
- with the same block address of first buffer. This block address must be even.
- lying at successive (modulo 24) Y addresses.

Figure 16 : Logical to Physical Address Transcoding Performed on-chip



X AND Y CONDITION		PHYSICAL ADDRESS AM (3:10)							
		10	9	8	7	6	5	4	3
Y ⩾ 8	X5 = 0	b0	Y4	Y3	Y2	Y1	Y0	X4	X3
	X5 = 0	b0	0	0	Y2	Y1	Y0	Y4	Y3
Y0 = 0		b0	0	0	X5	X4	X3	0	0

Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer or row buffer structure. See Figure 15 for pointer incrementation implied by these data structures.

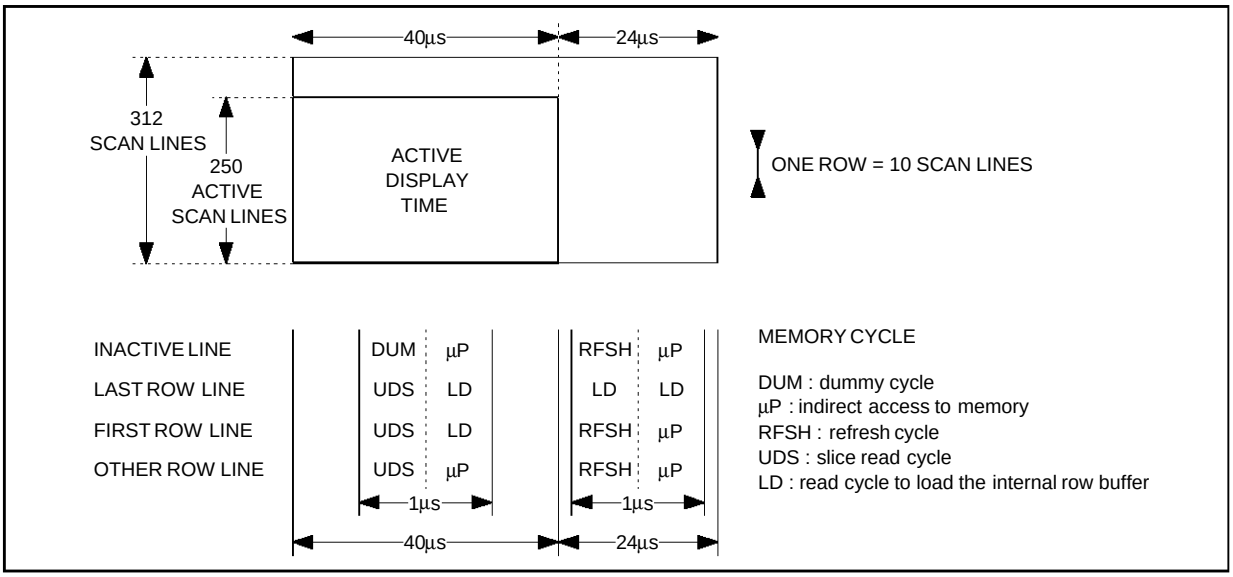
Memory Time Sharing (see Figure 17)

The memory interface provides a 500ns cycle time at f_{IN} = 12MHz. That it to say a 2 Mbyte/s memory bandwidth is shared between :

- reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- reading user defined characters slices from memory (1 byte each µs),
- indirect microprocessor read or write operation,
- refresh cycles to allow DRAM use, with no overhead.

A fixed allocation sheme implements the sharing. During these lines, no microprocessor access is provided for 104µs ; this holds too when no user defined character slices are addressed.

Figure 17 : Memory Cycle Allocation (12MHz operation).



Notes :
1. Dumming cycles are read cycles at dummy addresses.
2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM (0:7) cycle through its 256 states in less than 1ms.
3. The microprocessor may indirectly access the memory once every µs, except during the first and the last line of a row, when the internal buffer must be reloaded.

SCREEN FORMAT AND ATTRIBUTES OUTPUTS CONFIGURATION

The screen format and attributes are programmed through 5 indirectly accessible registers : ROR, TGS, PAT, MAT, and DOR. IND command allows accessing to these registers. TGS is also used to select the timing generator options (see Figures 18a and 18b).

Row And Character Code Format : TGS (6:7)

Two row formats and 4 character code formats are available but cannot be mixed in a given screen.

Timing Generator And Configuration Options : TGS (1:5)

TGS1 = 0 : noninterlaced mode, 312 lines/frame.
TGS1 = 1 : interlaced mode, 312.5 lines/frame.
TGS (2,3) : input synchronization configuration.

The SYNC input may be interpreted as a synchronization signal or as a general purpose input port, which state can be read by the microprocessor in the status register (bit 2). Alternatively, the vertical synchronization output from the timing generator can be read in the same register.
The composite incoming SYNC IN signal is separated into two internal signals :
- Vertical Synchronization In (VSI)
- Horizontal Synchronization In (HSI)

TGS3 = 1 enables VSI to reset the internal line count : SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 0 to 1, the line count is reset at the end of the current line.

TGS3 = TGS2 = 1 enables HSI to control an internal digital PLL : HSI and on-chip generated H. SYNC OUT are considered as in phase if their leading edges match at plus or minus 1 clock period. When they are out of phase, the line period is lenghtened by 1 clock period (80 ns at 12 MHz).
Screen Format Table resumes the different combinations.

TGS (4,5) : output configuration
Three output pins may be configured to output either video signals or general purpose output ports. The Screen Format Table summarizes the possible configurations, with the following definitions :

R, V, B : Red, Green and Blue Video components
I : Insert signal
HVS : Composite H and V synchro output
P1, P2 : General purpose output ports

PAT2 gives the value of P1, PAT7 gives the value of P2 : a logical ”1” will cause a ”high” on the corresponding output, while a ”0” results in a ”low”.

Figure 18a : Screen Format Table

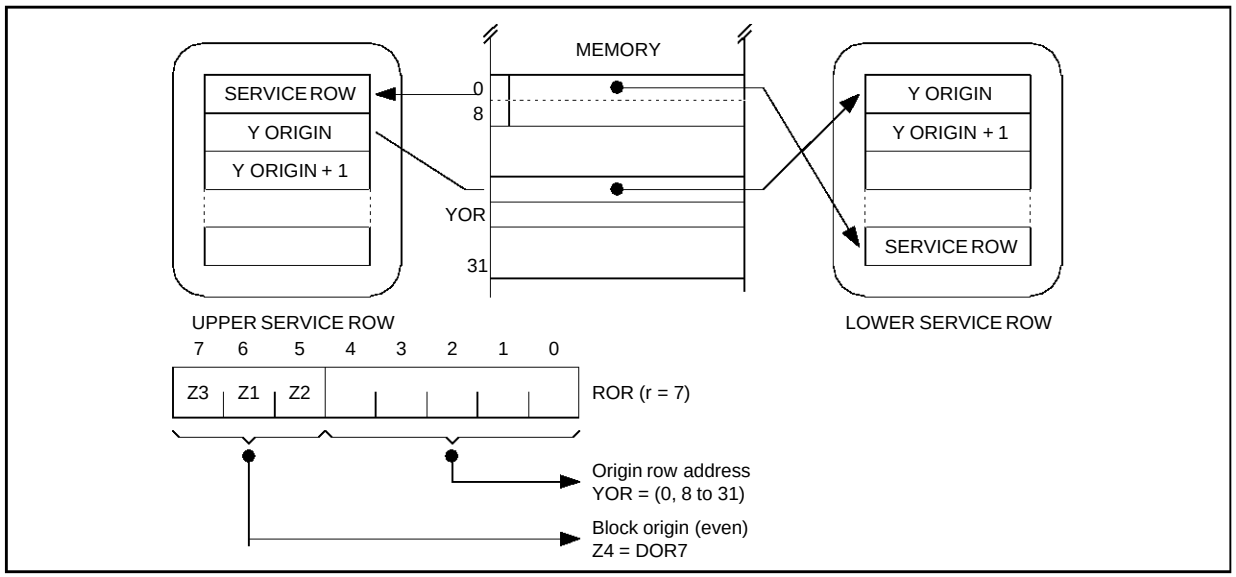
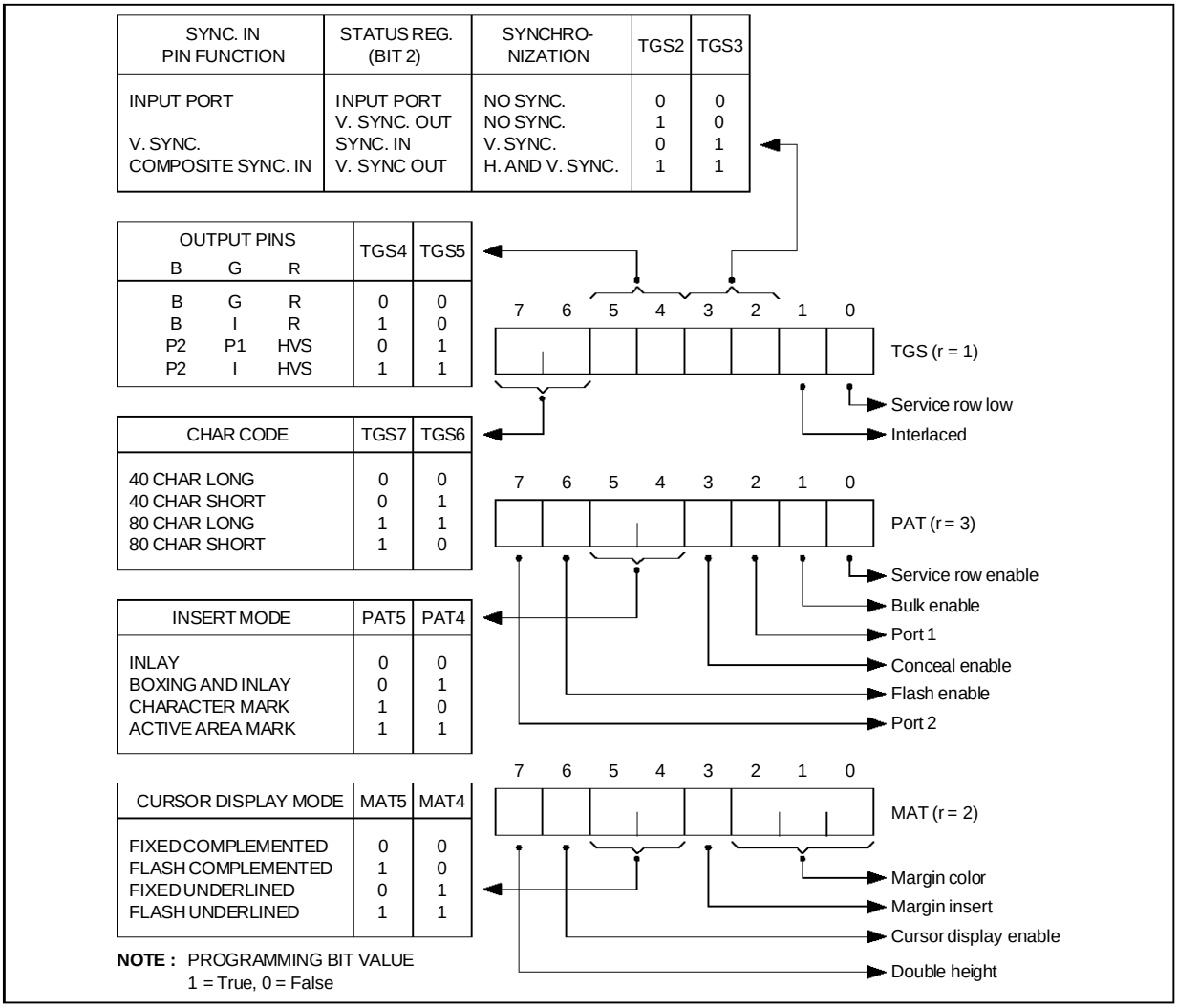


Figure 18b : Screen Format Table



Screen Partition, Page Pointer ROR (see top of the Screen Format Table)

The screen is partitioned in three areas :
- The margin
- The service row
- The bulk or remaining rows

MAT (0:3) declares the color of the margin and the value IM of its insert attribute.

DOR7 and ROR register point to the page to be displayed : DOR7 gives the MSB of the Z address, ROR (7:5) three next bits, the LSB is implicitly Z0 = 0 (the page block address must be even). YOR (= ROR (4:0)) gives the first row to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

Service Row : TGS0 ; PAT0

The 10 scan line service row can be displayed at the top or the bottom of the screen, depending on the value of TGS0. The service row is fetched from the origin block at Y = 0 ; it does not roll ; it may be disabled by PAT0 = 0 ; it is then displayed as a margin extension.

Bulk : PAT1 ; MAT7

The bulk is displayed for 240 scan lines. Each row buffer is usually displayed for 10 scan lines. However, MAT7 = 1 doubles this figure : then every character appears in double height (double height characters are quadrupled).
PAT1 = 0 disables the bulk. When disabled, the corresponding scan lines are displayed as a margin extension.

Cursor : MAT (4:6)

To be displayed with the cursor attribute, a character must be pointed by the main pointer (R6, R7) and MAT6 must be set. The cursor attributes are given by MAT (4,5) :
- Complementation :
  The R, G, B or each pixel is logically negated : R, G, B $\rightarrow$ $\overline{R}$, $\overline{G}$, $\overline{B}$
- Underline :
  The underline attribute is negated
- Flash :
  The character is periodically displayed with, then without the cursor attribute (50%/50% $\approx$ 1 Hz).

Flash Enable (PAT 6) **- Conceal Enable** (PAT3)

Any character flashing attribute is a "don't care" when PAT6=0. When PAT6 = 1, a character flashes if its flashing attributes is set. It is then periodically displayed as a space (50%/50% $\approx$ 0.5Hz).
PAT3 is a 'don't care" for 80 char./row formats.
When any 40 char./row format is in use :
- if PAT3 = 0, the conceal attribute of any character is a "don't care"
- if PAT3 = 1, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

Insert Modes : PAT (4:5)

These modes make sense only if the insert signal I is available on the G pin, that is to say when TGS4 = 1.
During retrace, margin and extended margin periods, the I signal outputs the value of the insert margin attribute : I = IM = MAT3.
During active line period, the I output is controlled by the insert mode, and I1 and I2, the insert attributes of each characters. The I output may have several uses : (See Figure ???).
- As a margin/active area signal in the Active Area Mark mode
- As a character per character marker signal in the Character Mark mode
- As a video mixing signal in the other modes, provided that the TS9347 has been vertically and horizontally synchronized with an external video source : the I output allows mixing TS9347 video output (I = 1) and external video signal (I = 0). This mixing may occur for the complete character window (Boxing mode) or only for the foreground pixels (Inlay mode).

Video Output during Active Periods

Insert Mode	I1	I2	Char. Levels Pixels	I	Video Output	Comments
Active Area Mark	-	-	-	1	Unchanged	
Character Mark	0	-	-	0	Unchanged	
	1	-	-	1	Unchanged	
Inlay	0	-	-	0	Black	Non insert
	1	-	Background	0	Black	
	1	-	Foreground	1	Unchanged	Inlaid
Boxing and Inlay	0	-	-	0	Black	Non inserted
	1	0	-	1	Unchanged	Boxed
	1	1	Background	0	Black	
	1	1	Foreground	1	Unchanged	Inlaid

9347-14.TBL

40 Char/row Character Codes

To display pages in 40 character per row format, one out of two character code formats must be selected :

- Long (24 bits) code : all parallel attributes.
- Short (16 bits) code : mix of parallel and latched attributes.

Short codes are translated into long codes by the TS9347 during the internal row buffer loading process. The choise of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

Long Codes

This is the basic 40 char/row code. Each 8 pixel x 10 lines character window on the screen is associated with a 3-byte code in memory, namely the C, B, and A bytes (Figure 19). A row on the screen is associated with a 120 byte row buffer in memory.

3-BYTE CODE STRUCTURE

1. C7 is a don't care. up to 128 characters may be addressed in each set. each user definable set holds only 100 characters : C-byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B (3:7) give the type and the set number of the character.
3. When I2, U, L are not programmable, the default value of these attributes is 0.
4. Character code byte a defines a two color set giving directly (Table 3) the two values (B1, G1, R1) and (B0, G0, R0) respectively affected to the 1's and the 0's of the character pattern. the negative attribute, when set, exchanges the two values.

Figure 19 : 40 Character Long Codes

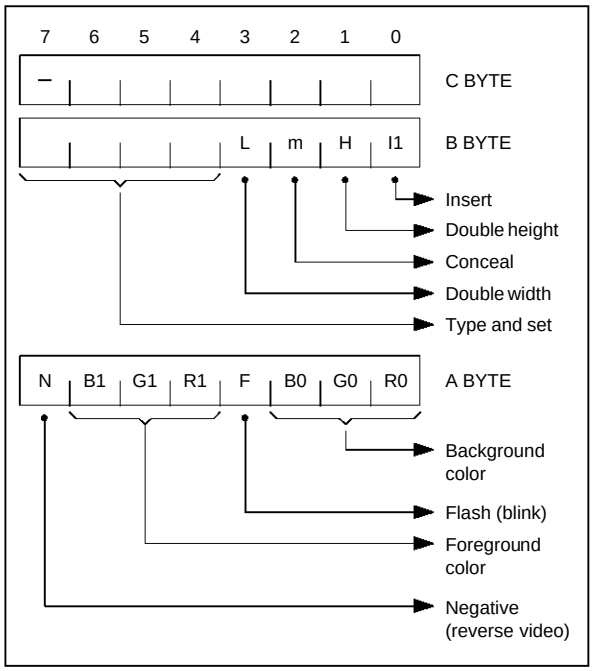


Table 2

Type and Set B (3:7)					Number of Character Per Set	Set Name	Set Type	Cell Location
B7	B6	B5	B4	B3	C (0:6)			
0	I2 I2	1 1	0 1	L L	128 STANDARD MOSAIC 32 COMPLEMENT. CELLS	G10 GOE	SEMI GRAPH	ON CHIP ROM
	I2	0	U	L	128 ALPHANUMERICS	G0	ALPHA	
1	0	0	U	L	100 ALPHA UDS	G'0		EXTERNAL RAM
	0	1	0	L	100 SEMI-GRAPHICS UDS	G'10	SEMI GRAPH	
			1	L	100 SEMI-GRAPHICS UDS	G'11		
	1	X	X	X	800 SEMI-GRAPHICS UDS	Q0:7		

9347-15.TBL

L = Double width U = Underlined

Notes: 1. Double height, double width : a correct operation assumes that the same character code had been repeated in the page memory (Twice for double height or double width, four times for double size).
2. Double height : each slice of the character is repeated : twice to get a 8 x 20 pattern. However for the alphanumeric characters, scheme is slightly different : the upper slice (SN = 0) is tripled, the next (SN = 1 to 8) are doubled, and the last (SN = 9) is displayed only once.

Table 3 : Coloring a Character

B	G	R	Color Value
0	0	0	BLACK
0	0	1	RED
0	1	0	GREEN
0	1	1	YELLOW
1	0	0	BLUE
1	0	1	MAGENTA
1	1	0	CYAN
1	1	1	WHITE

9347-16.TBL

Table 4 : Shifting a Slice

7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0

---------- →
Shift Direction : LSB First
1 = Foreground
0 = Background

9347-17.TBL

Short Codes

These 16-bit codes achieve memory saving whith some penalties :

- Q0 to Q7 and GOE cannot be reached.
- Some attributes are latched and can be changed only while displaying a space (delimitor code).

They are fully compatible with EF9345 (binary code and display interpretation) if the I2 attribute is given the value 0.

Figure 22 gives the short to long translation process which occurs for each row - while loading the internal row buffer - before display.

HANDLING SHORT AND LONG CODES

The TLM, TLA, TSM, and TSA, commands allow an easy X, Y random or an X sequential access to/from the microprocessor from/to a memory row buffer (see Figures 20 and 21).

User Defined Character Generator In Memory : DOR REGISTER

With 40 char./row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus, a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (Figure 23).

The cells of one given character set should be layed in one block.

Up to 100 character cells may be addressed in each set.

The location in memory, where to fetch the sets in use, are declared by DOR register (Figure 24).

For each type of set, it gives the MSB(s) of the Z block address. TS9347 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. SN is derived from the scan line rank in the row and the double height status.

Figure 20 : Long Codes in Memory Triple Row Buffer

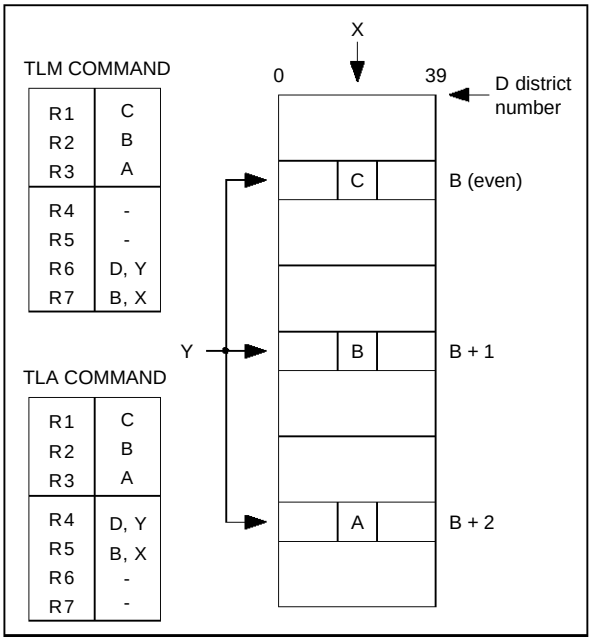


Figure 21 : Short Codes in Memory Double Row Buffer

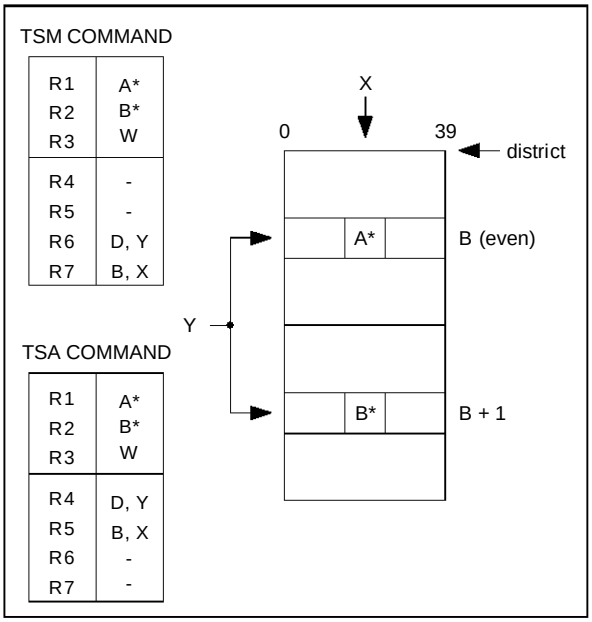
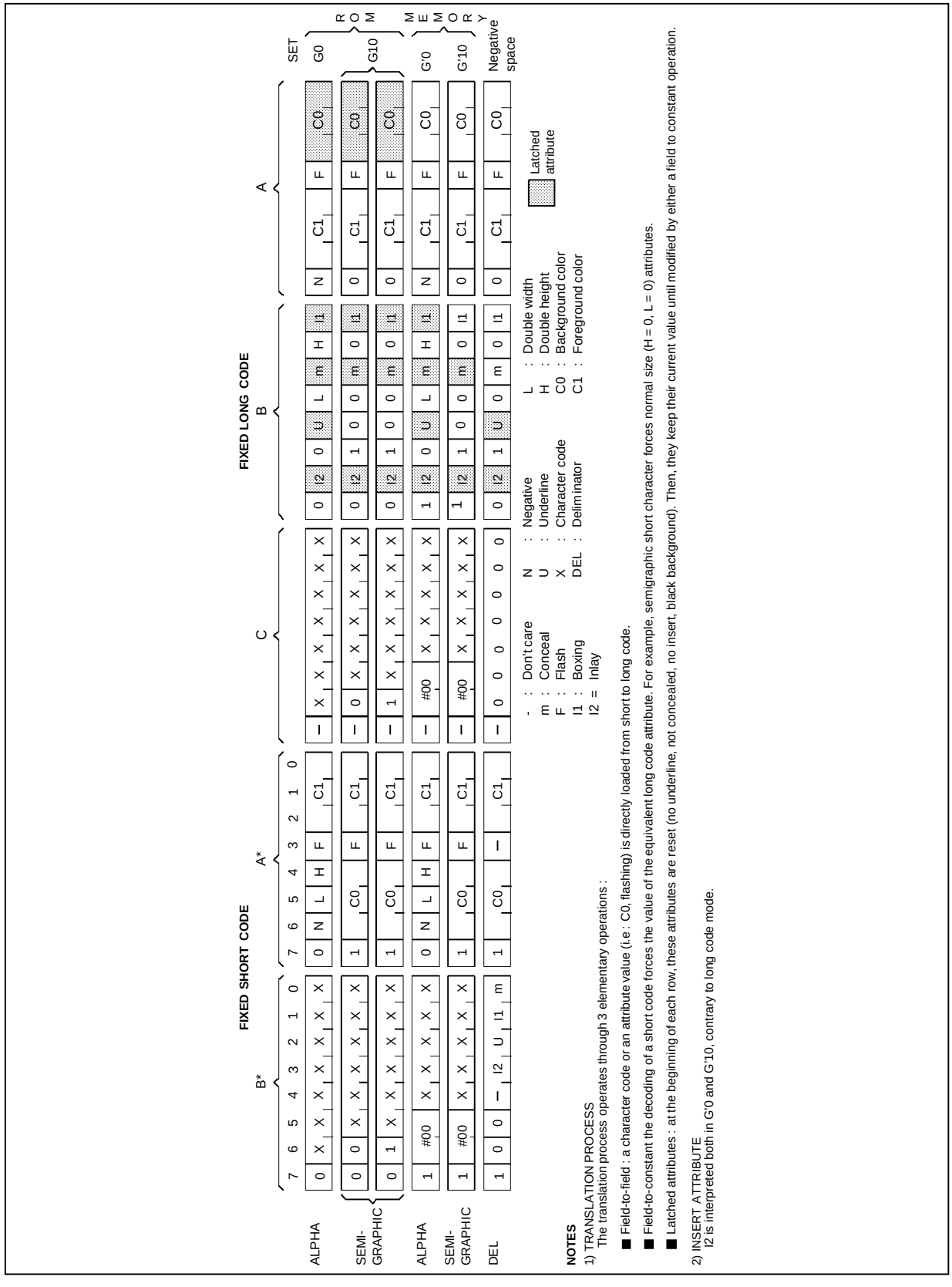


Figure 22 : Fixed Short Code to Fixed Long Code Translation



NOTES

1) TRANSLATION PROCESS
The translation process operates through 3 elementary operations :

- Field-to-field : a character code or an attribute value (i.e : C0, flashing) is directly loaded from short to long code.
- Field-to-constant the decoding of a short code forces the value of the equivalent long code attribute. For example, semigraphic short character forces normal size (H = 0, L = 0) attributes.
- Latched attributes : at the beginning of each row, these attributes are reset (no underline, not concealed, no insert, black background). Then, they keep their current value until modified by either a field to constant operation.

2) INSERT ATTRIBUTE
I2 is interpreted both in G'0 and G'10, contrary to long code mode.

9347-27.EPS

Figure 23 : Packing Uds Cells in Memory

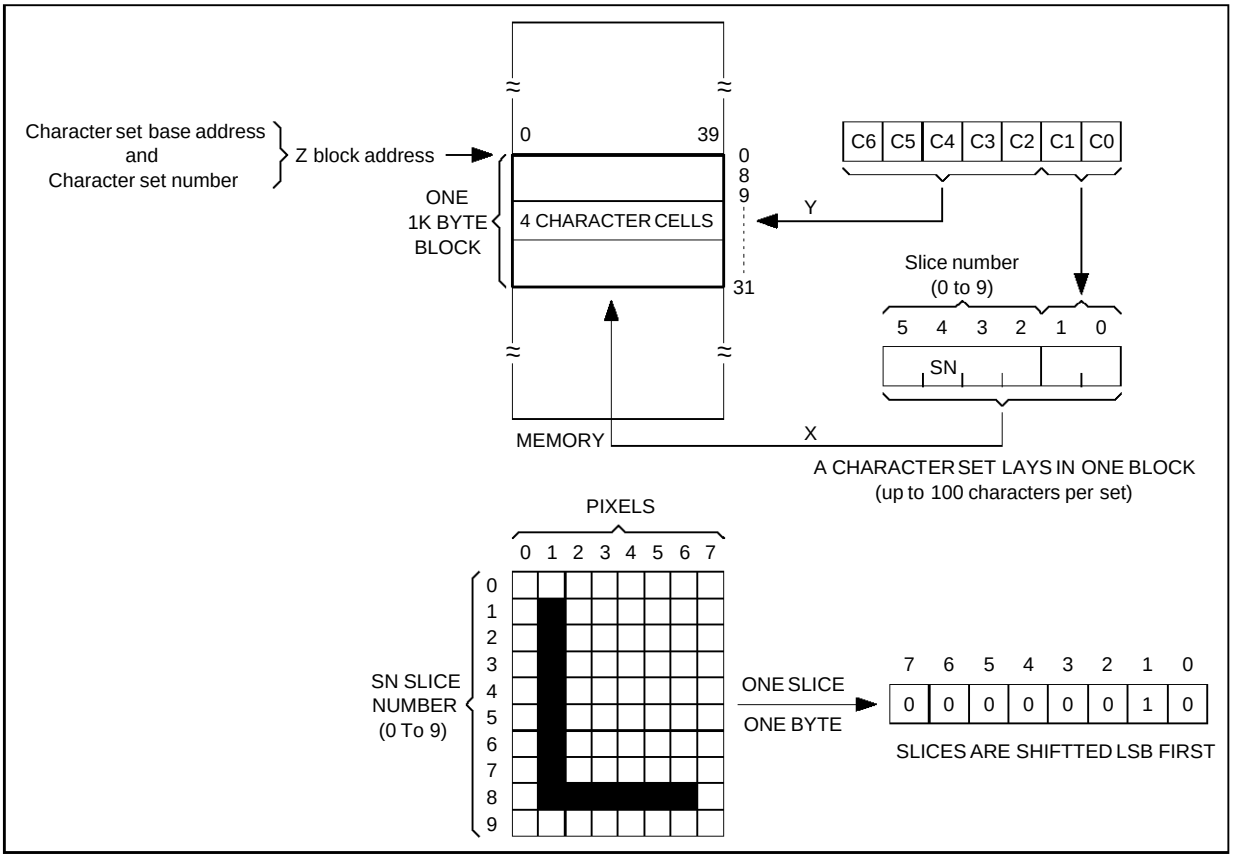
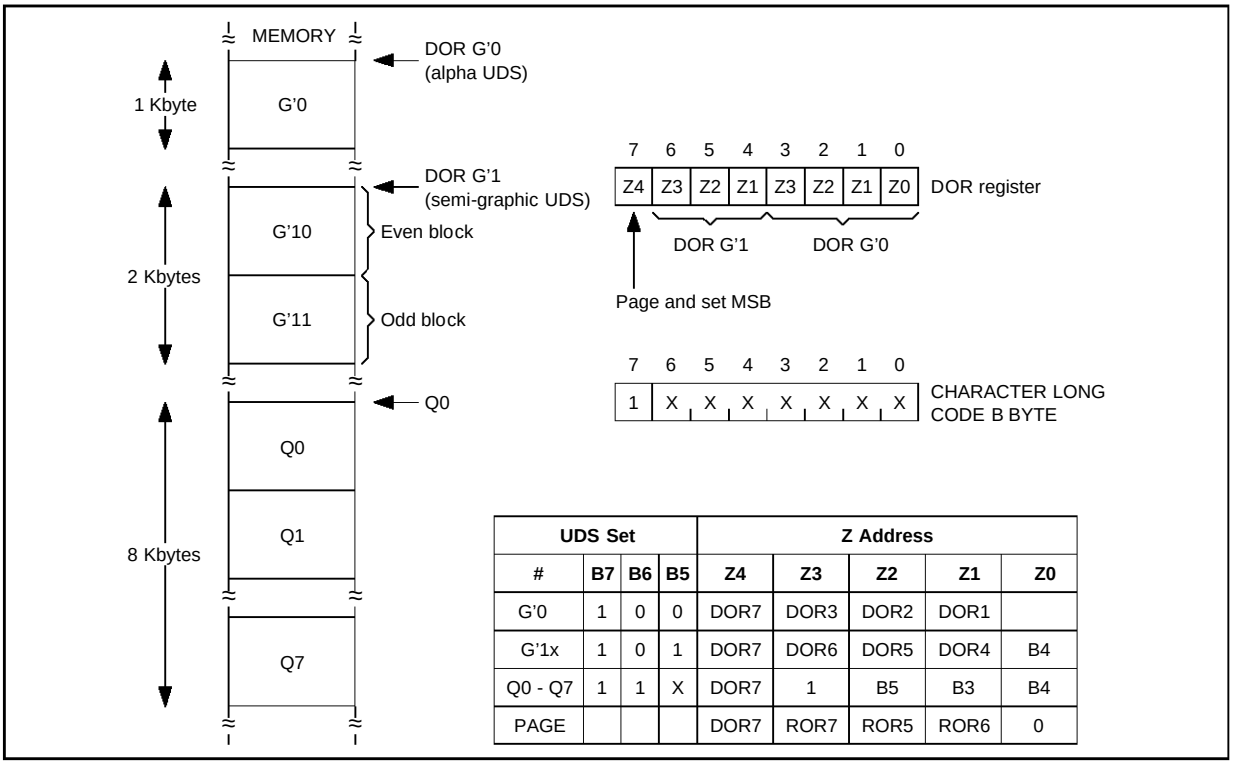


Figure 24 : UDS Fetch to Display



UDS Set				Z Address				
#	B7	B6	B5	Z4	Z3	Z2	Z1	Z0
G'0	1	0	0	DOR7	DOR3	DOR2	DOR1	
G'1x	1	0	1	DOR7	DOR6	DOR5	DOR4	B4
Q0 - Q7	1	1	X	DOR7	1	B5	B3	B4
PAGE				DOR7	ROR7	ROR5	ROR6	0

Loading User Defined Character Set

Before loading a character set into RAM, the user must

- Assign a name to the set :
  G'_0, G'_{10}, G'_{11}, or Q_{0-7}
- Assign a character number to each character belonging to this set. Character numbers range from 0 to 3 and 32 to 127.
  It is binary coded into 7 bits C (0.6) - C (0.6) will be loaded later into a C byte character code in order to display the character.
- A pointer to a character slice in memory is then manufactured from
  the character number C (0.6),
  the slice number SN (0.3),
  the bloc number assigned to the set Z (0.4)

Note : Different sets may be mixed in the same block, as long as the character have different code numbers.

Figure 25 : Accessing a Character Slice in Memory

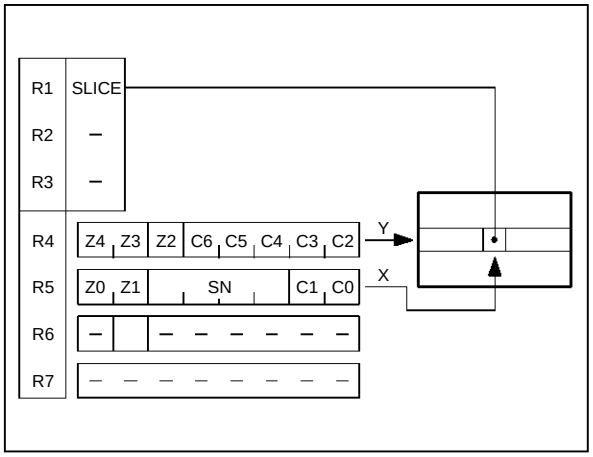


Figure 25 shows how to proceed with the auxiliary pointer and the TBM and TBA commands.

Note : The main pointer may be also used. When sequentielly accessing slices of a given character, auto incrementation is helpless.

On-chip Character Generator

- G0 and GOE are common to 40 and 80 char./row modes (Figure 26 and Figure 36).
- G10 is the standard mosaïc set for videotex (Figure 27).
- GOE cannot be reached from the 16 bit short codes (Figure 28).

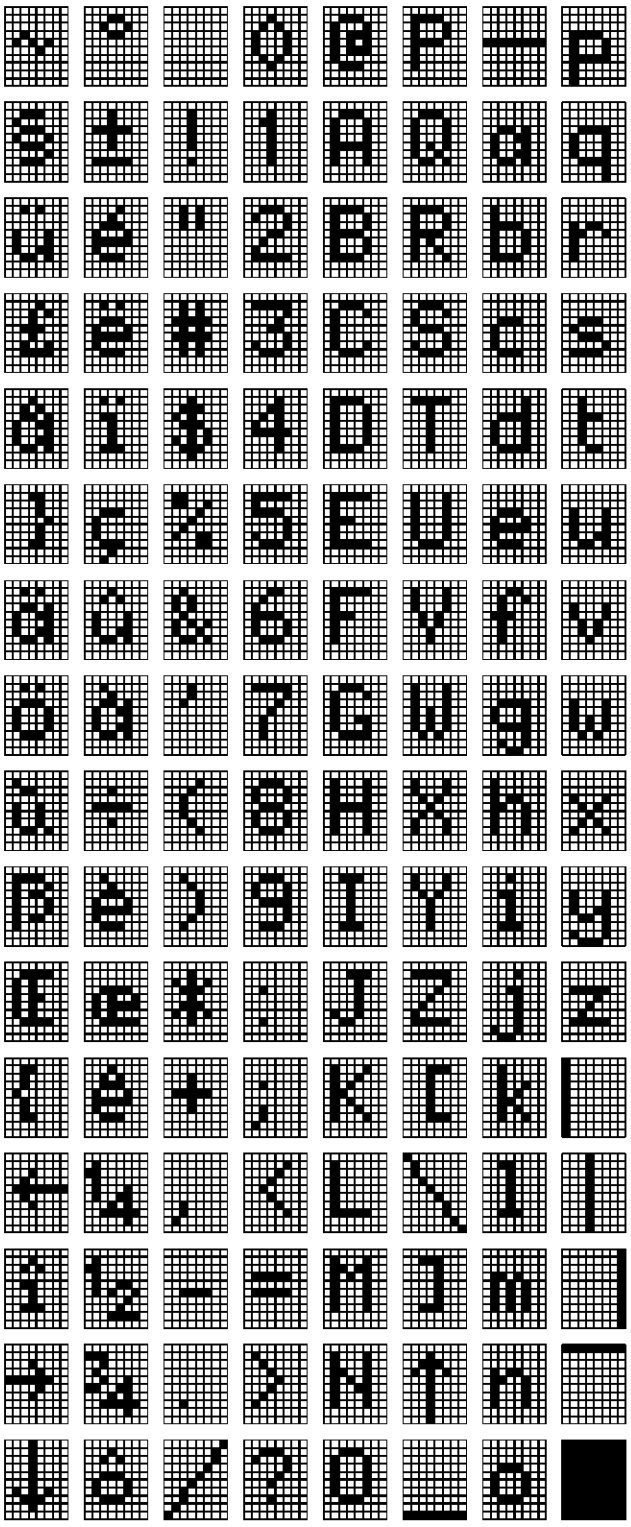
Displaying the Attributes

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :
   - Underline or underline cursor : foreground forced on the last slice (SN = 9).
   - Flash : background periodically forced on the whole window (≈ 0.5 Hz). The phase depends on the negative attribute.
   - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
   - Negative : exchange the background and foreground color values when set.
   - Coloring.
3. Basic pixel shift frequency : f_{CLK} x 2/3 = 8 to 10MHz

Figure 26 : G_O Alphanumeric Character Set in 40 Character/Row Mode–TS9347.

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1



9347-31.EPS

Figure 27 : G_{10} Semigraphic Character Set.

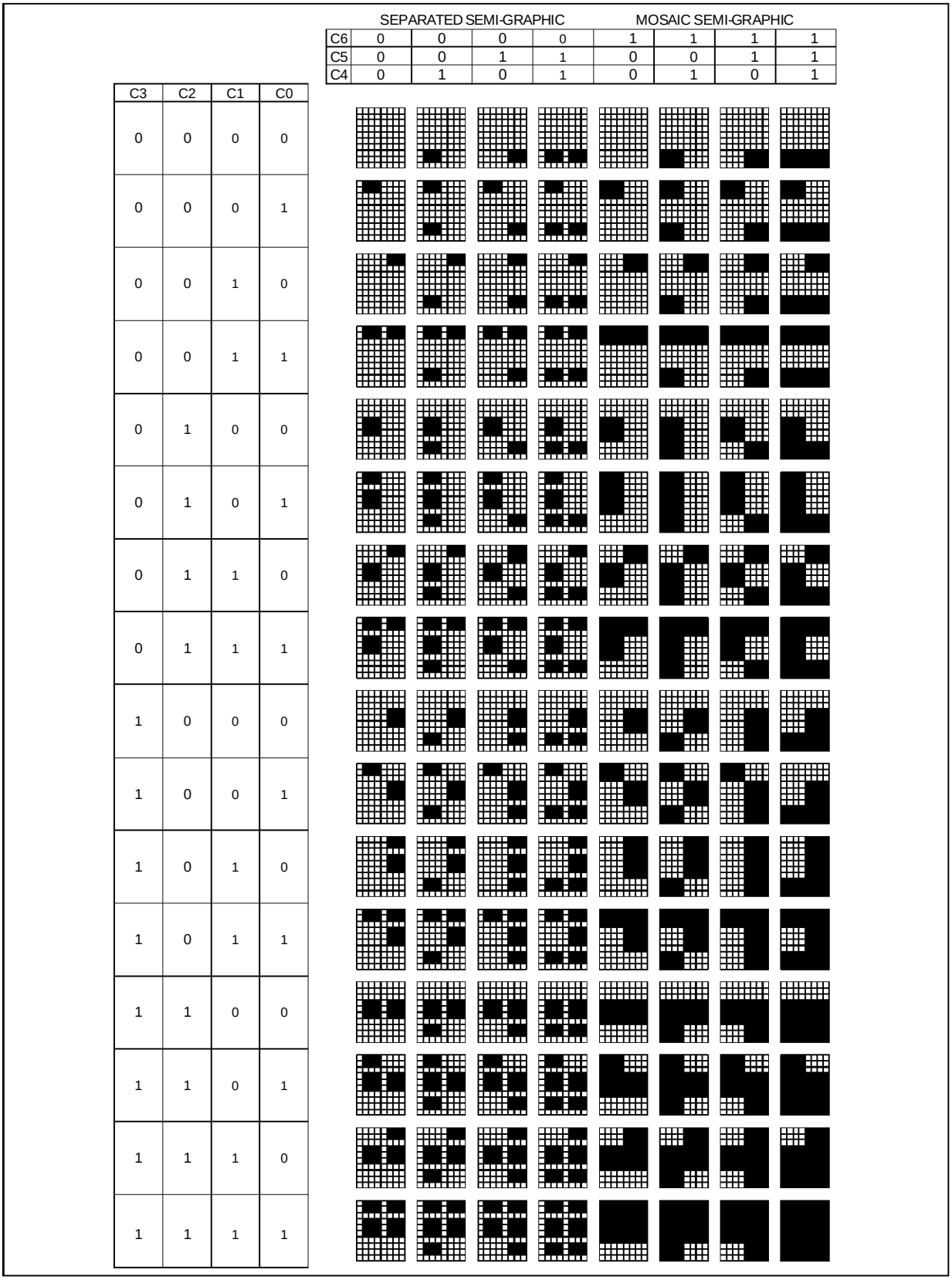
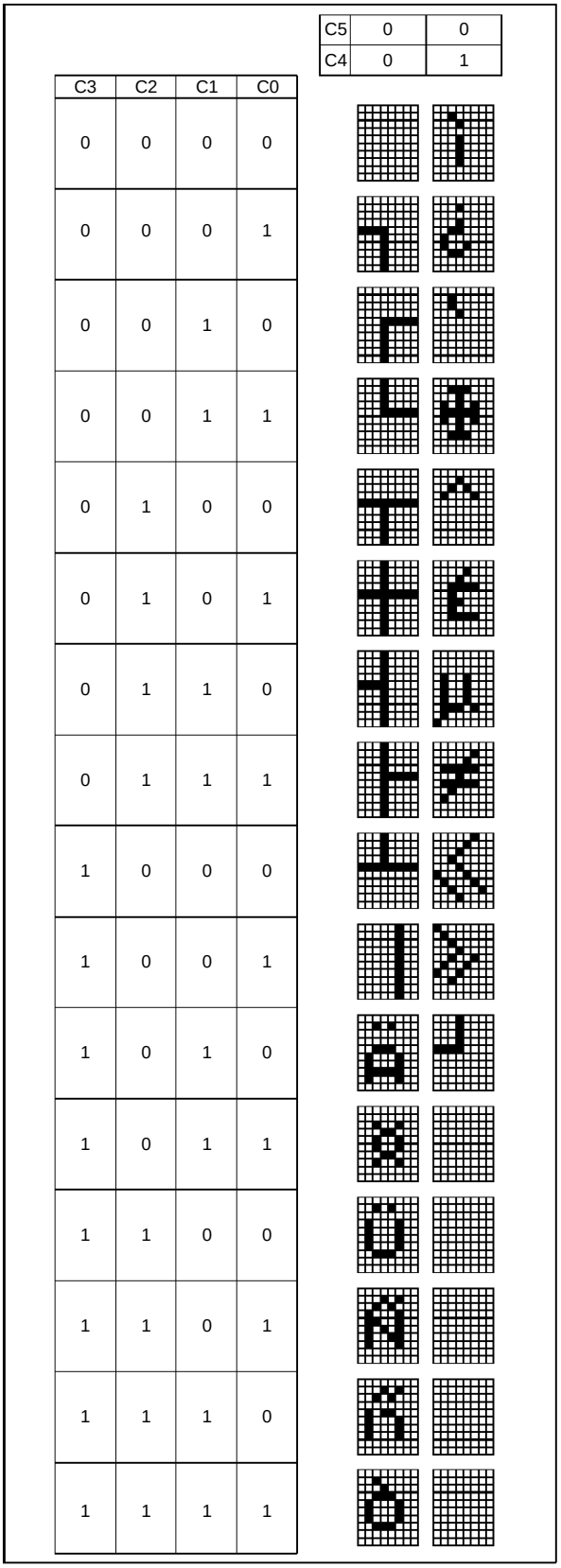


Figure 28 : GOE Extension Character Set



80 CHAR / ROW CHARACTER CODES

To display pages in 80 character per row format, one of two character code formats must be selected :

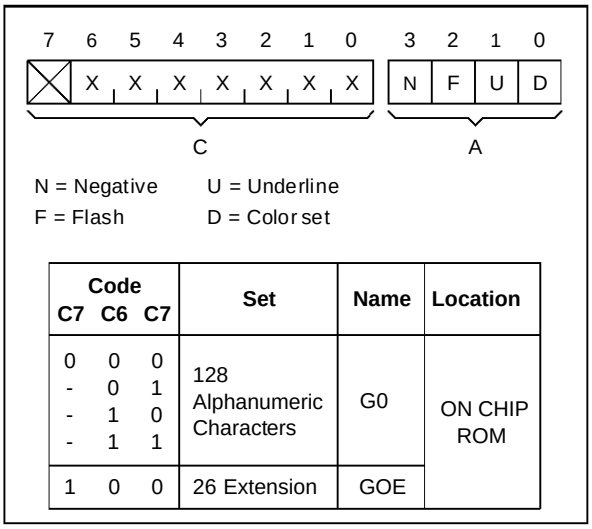
- Long (12 bits) code : 4 parallel attributes
- Short (8 bits) code : no attribute.

Both formats address the on-chip G_0 and GOE sets (154 characters 6 x 10) sets. None allows UDS addressing.

Long Codes

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (Figure 29).

Figure 29 : 80 Char/Row Character Code



Code C7	C6	C7	Set	Name	Location
0	0	0	128 Alphanumeric Characters	G0	ON CHIP ROM
-	0	1			
-	1	0			
-	1	1			
1	0	0	26 Extension	GOE	

Short Codes

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble positive, not underlined, not flashing.

Packing The Codes In Memory

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (Figure 30). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

Access To The Codes In Memory

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A

nibble is repeated in the R3 register (Figure 31). Dedicated auto-incrementation is also performed when required.
KRS command does a similar job the short codes (Figure 32).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (Figure 33). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

Figure 30 : 80 Char / Row Code Packing

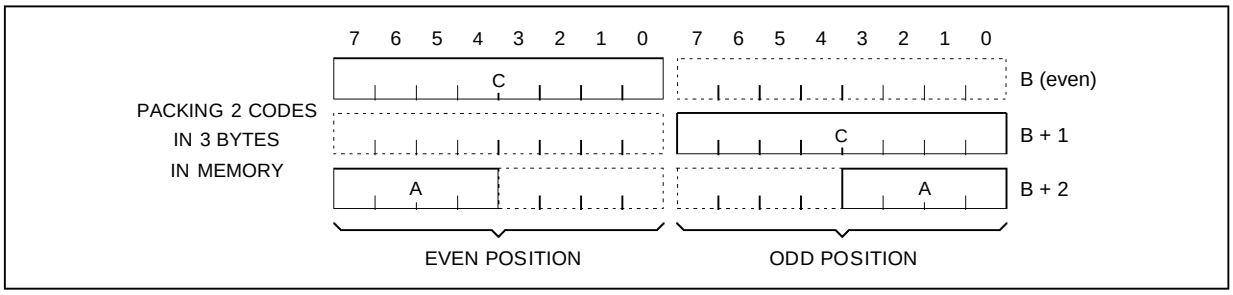


Figure 31 : KRL Command : Sequential Access to Long Codes

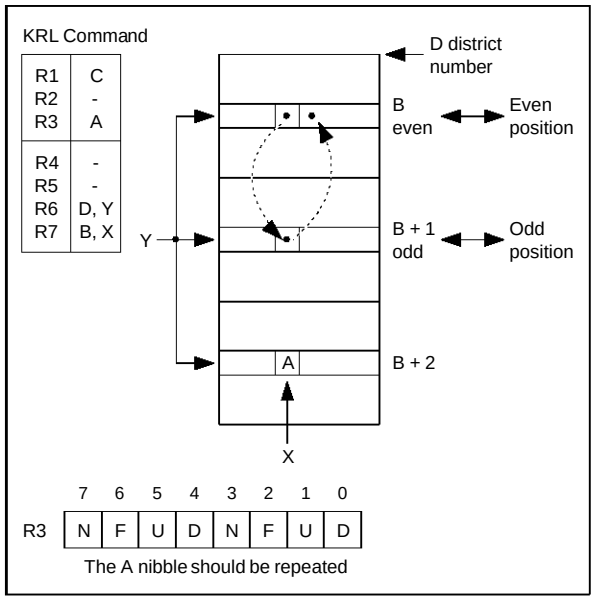


Figure 32 : KRS Command Sequential Access to Short Codes

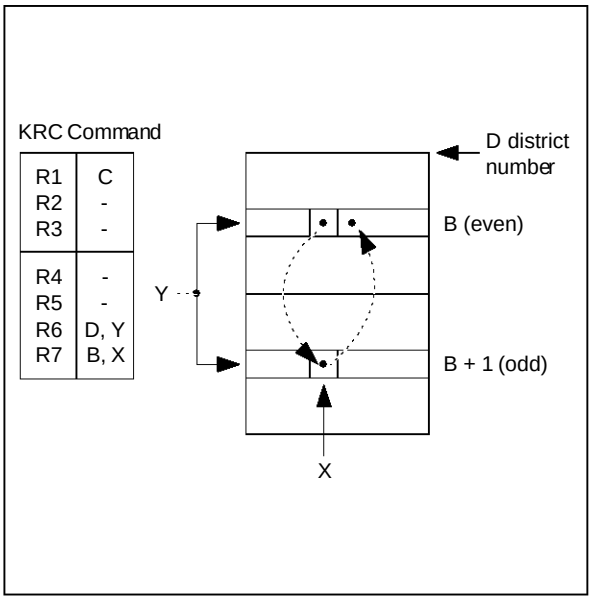
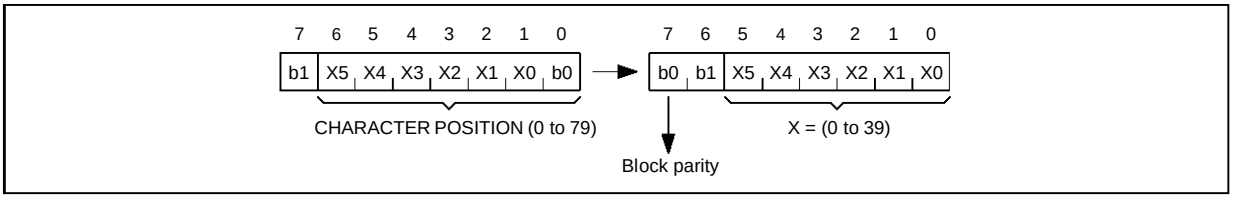


Figure 33 : Transcoding an Horizontal Screen Location into a R7 Pointer



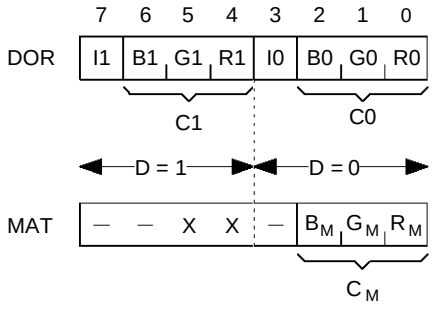
Displaying The Attributes : DOR REGISTER (see Figure 34)

Short code character are not flashing, not underlined and ”positive”.

The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (SN = 9).
- Flash : background is periodically (0.5Hz - 50%) forced on all the window. The phase depends on the negative attribute.
- Color select : a ”positive” character is displayed with a background color same as the margin color. The foreground color is selected in DOR register by the D attribute.
- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : The D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section).

Figure 34

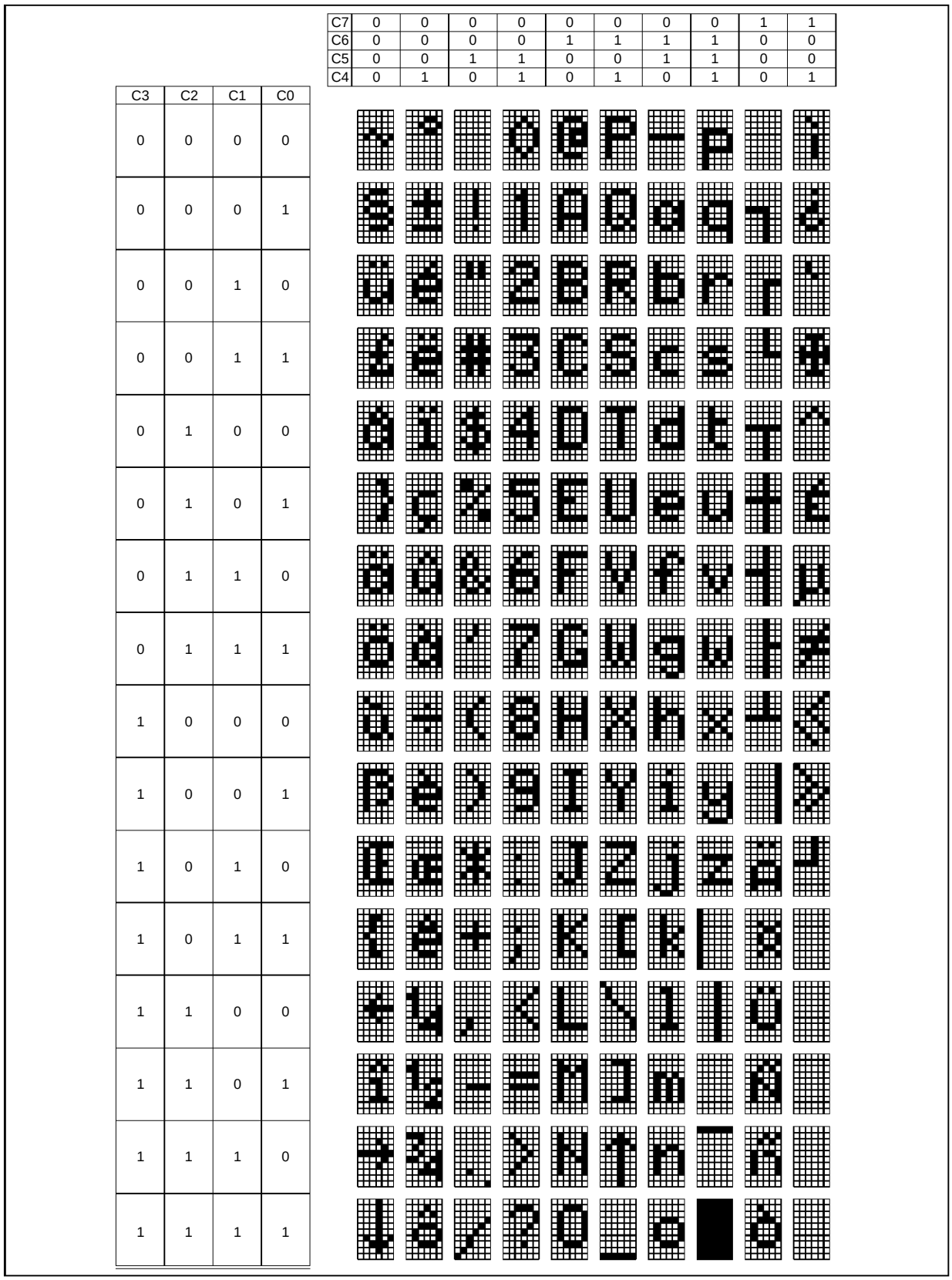


D	N	Background Color	Foreground Color	i
0	0	C_M	C0	i0
0	1	C0	C_M	i0
1	0	C_M	C0	i1
1	1	C0	C_M	i1

The pixel shift frequency is f_{CLK} (12 to 15MHz)

9347-39.EPS

Figure 35 : G_{OE} Alphanumeric Character Set in 80 Character/Row Mode - TS9347



MICROPROCESSOR ACCESS COMMANDS

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :

- to/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- to/from the dedicated memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

Address Phase

The falling edge of AS latches the AD (0.7) bus state and CS signal into the temporary A address register (Figure 36).

- A (0:2) = i
  This register index designates one out of 8 direct access registers R_i.
- A3 = XQR
  This is the execution request bit.
- A (4:7) = ASN
  This is the Auto-Selection Nibble.
- A8 = $\overline{LCS}$
  This is the latched value of $\overline{CS}$ input pin.

TS9347 is selected when the following condition is met : ASN = 2 (Hexa) and $\overline{LCS}$ = 0.

Therefore, TS9347 is mapped in the hexadecimal microprocessor addressing space from XX20 to XX2F, where XX is up to the user. When TS9347 is not selected, its AD bus pins float and no register can be modified (see Figure 37)

Data Phase - Registers

When TS9347 is selected and while AS input is low, the R_i register is accessed.
R0 designates a write-only COMMAND register or a read-only STATUS register.
R1 to R7 hold the arguments of a command. They are read/write registers.
R1, R2, R3 are used to transfer the data.
R4, R5 hold the Auxiliary Pointer (AP).
R6, R7 hold the Main pointer (MP).
(See Figure 36).

Command Register

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see COMMAND TABLE).

Type

There are 3 groups of command :

- The IND command which gives access to on-chip resources,
- The character code transfer commands,
- The general purpose commands.

Parameters

R/$\overline{W}$: Direction
  1 : to DATA registers (R1, R2, R3)
  0 : from DATA registers.

r : Internal resource index (see Figure 38)

I : Auto-incrementation
  1 : with post auto-incrementation
  0 : without auto-incrementation.

p : Pointer select
  1 : auxiliary pointer
  0 : main pointer

s, $\overline{s}$: Source, destination select
  01 : source : MP ; destination : AP
  10 : source : AP ; destination : MP

$\overline{a}$, a : Stop condition
  01 : stop at end of buffer
  10 : no stop.

Figure 36 : Direct Access Registers

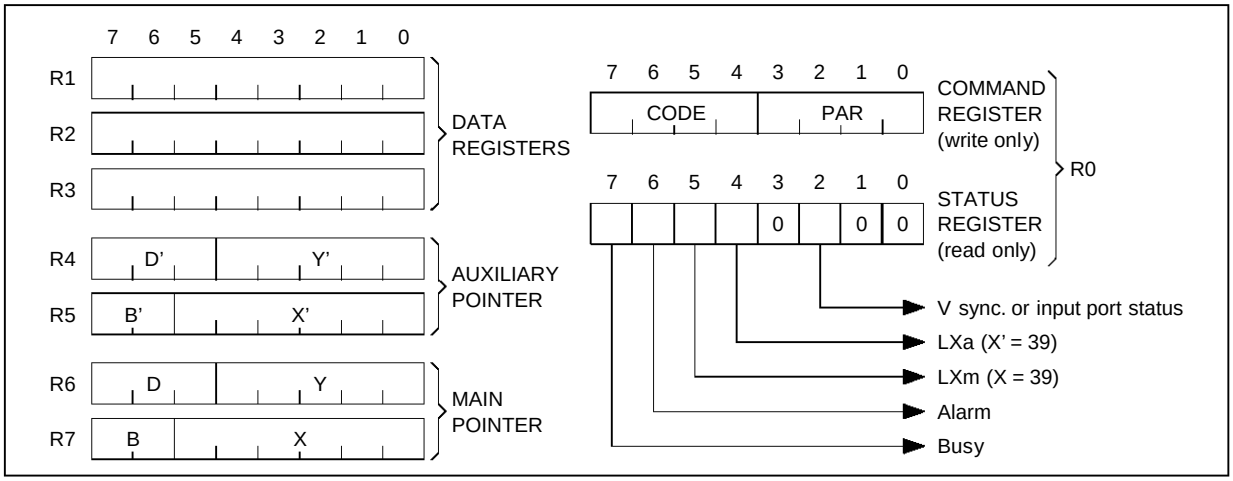


Figure 37

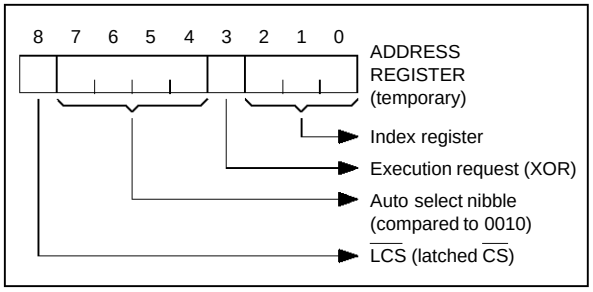
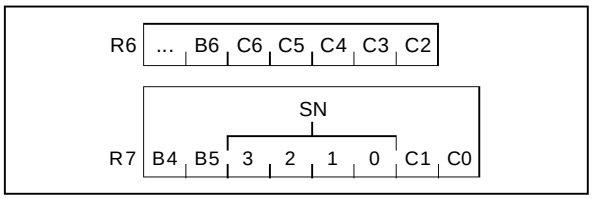


Figure 38 : Indirect on–chip Ressource Access



STATUS REGISTER

This is a read-only, direct access register.

S7 : BUSY — BUSY is set at the beginning of any command execution. It is reset at completion.

S6, S5, S4 : AI, LX_m, LX_a — LX_m or LX_a is set when respectively the main pointer or the auxiliary pointer holds X = 39 before a possible incrementation.
The alarm bit S6 is set when LX_m or LX_a is set and an incrementation is performed after access.

S2 : Gives the vertical synchronization signal state, or the input port value. This is maskable by the VRM command. In this case, its values is 0.

S3 = S1 = S0 = 0 Not used.

S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.

Notes on Command Execution

1. The execution of any command starts at the trailing edge of DS when (and only when) :
   - TS9347 has been selected,
   - XQR has been set,

   at the previous AS falling edge.
   This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.
2. At power on, the busy state is undeterminated. It is recommanded to load first a NOP command with XQR = 1 before any effective command.
3. While Busy is set, the current command is under execution. Register access is then restricted.
   Register access with XQR = 0
   - Read STATUS is effective.
   - Write COMMAND or any other register access are ineffective.

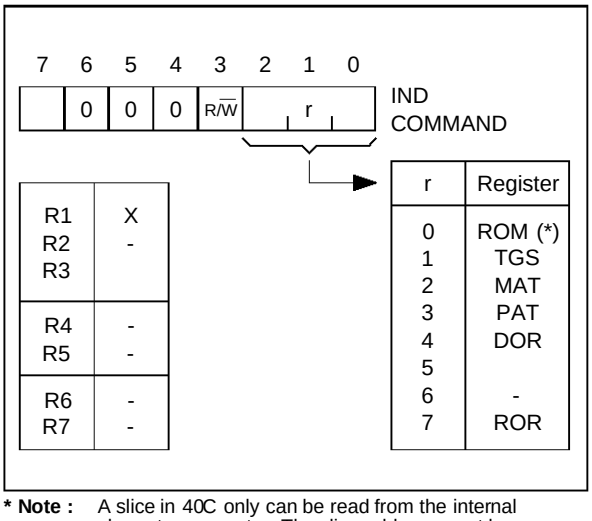
   That is to say, the microprocessor reads undertermined values and may not modify a register.
   Register access with XQR = 1
   - Read STATUS or write COMMAND are effective,
   - Access to other registers is ineffective.

   However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).
4. Execution suspension
   The execution of any command (except VRM, VSM) is suspended during the last and first scan line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 208 memory cycle period. This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND Command (see Figure 38)

This command transfers one byte between R1 and an internal resource. The r parameter designates on on-chip indirect register.

Figure 39



*** Note :** A slice in 40C only can be read from the internal character generator. The slice address must be initialized in R6, R7.

Character Code Access : TLM, TLA, TSM, TSA,KRL, KRS

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory.

TLM, TLA transfers 24 bits with Main/Auxiliary Pointer
TSM, TSA transfers 16 bits with Main/Auxiliary Pointer
KRL transfers 12 bits with Main Pointer
KRS transfers 8 bits with Main Pointer

Code packing, pointer and data structures are explained in the corresponding character code section.
When auto-incrementation is enabled, MP or AP is automatically updated after access so as to point to the next location.
This location corresponds to the next right position on screen. When last position (X = 39) is accessed, LX_m is set. When last position is accessed with auto-incrementation, alarm is also set. MP or AP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

General Purpose Access to a Byte : TBM, TBA

This command uses either MP or AP pointer.
When MP is in use, an overflow yields to a Y incrementation.

Move Buffer Commands : MVB, MVD, MVT

These are memory to memory commands which use R1 as working register.
MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word an 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter a = 1, the process stops when either source or destination buffer end is reached. If the parameter a = 0, the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

Miscellaneous Command : INY, VRM and VSM

INY command increments Y in MP.
VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor from the status register. After power on, the mask state is undetermined.

REGISTER - MAP

Figure 40a

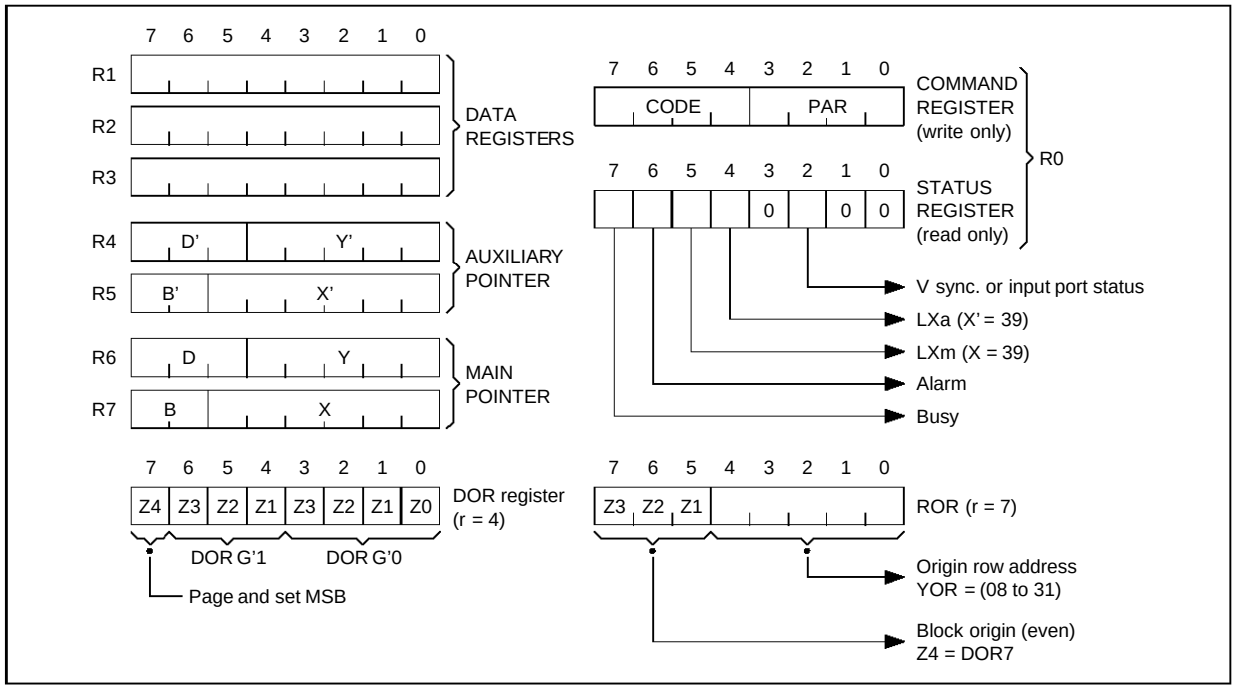


Figure 40b

SYNC. IN PIN FUNCTION	STATUS REG. (BIT 2)	SYNCHRO-NIZATION	TGS2	TGS3
INPUT PORT	INPUT PORT	NO SYNC.	0	0
	V. SYNC. OUT	NO SYNC.	1	0
V. SYNC.	SYNC. IN	V. SYNC.	0	1
COMPOSITE SYNC. IN	V. SYNC OUT	H. AND V. SYNC.	1	1

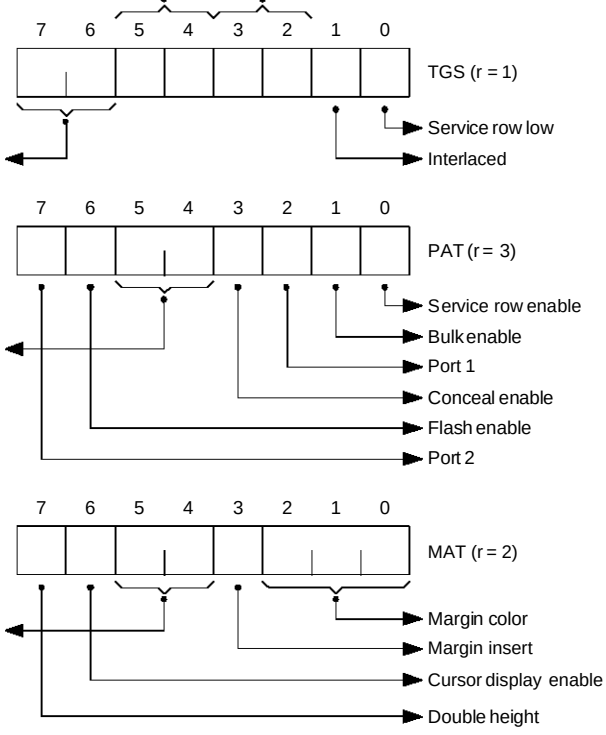
OUTPUT PINS B	G	R	TGS4	TGS5
B	G	R	0	0
B	I	R	1	0
P2	P1	HVS	0	1
P2	I	HVS	1	1

CHAR CODE	TGS7	TGS6
40 CHAR LONG	0	0
40 CHAR SHORT	0	1
80 CHAR LONG	1	1
80 CHAR SHORT	1	0

INSERT MODE	PAT5	PAT4
INLAY	0	0
BOXING AND INLAY	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

CURSOR DISPLAY MODE	MAT5	MAT4
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

NOTE : PROGRAMMING BIT VALUE
1 = True, 0 = False



9347-46.EPS

COMMAND TABLE

Type	Memo	Code				Parameter				Status			Arguments							Execution Time (1)	
		7	6	5	4	3	2	1	0	Ai	LX_m	LX_a	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R/$\overline{W}$	-	r	-	0	0	0	D	-	-	-	-	MP		2	3.5
40 Characters - 24 BIts	TLM	0	0	0	0	R/$\overline{W}$	0	0	I	X	X	0	C	B	A	-	-	MP		4	7.5
40 Characters - 24 BIts	TLA	0	0	1	0	R/$\overline{W}$	0	1	I	X	0	X	C	B	A	AP		-		4	7.5
40 Characters - 16 BIts	TSM	0	1	1	0	R/$\overline{W}$	0	0	I	X	X	0	A*	B*	-	-	-	MP		3	5.5
40 Characters - 16 BIts	TSA	0	1	1	1	R/$\overline{W}$	0	0	1	X	0	X	A*	B*	-	AP		-		3	5.5
80 Characters - 8 BIts	KRS	0	1	0	0	R/$\overline{W}$	0	0	I	X	X	0	C	-	-	-	-	MP		9	9.5
80 Characters - 12 BIts	KRL	0	1	0	1	R/$\overline{W}$	0	0	I	X	X	0	C	-	A	-	-	MP		12.5	11.5
Byte	TBM	0	0	1	1	R/$\overline{W}$	0	0	I	X	X	0	D	-	-	-	-	MP		4	4.5
Byte	TBA	0	0	1	1	R/$\overline{W}$	1	0	I	X	0	X	D	-	-	AP		-		4	4.5
Move Buffer	MVB	1	1	0	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 4.n	-
Move Double Buffer	MVD	1	1	1	0	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 8.n	-
Move Triple Buffer	MVT	1	1	1	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	W	-	-	AP		MP		(2) 2 + 12.n	-
Clear Page (4) - 24 Bits	CLL	0	0	0	0	0	1	0	1	X	X	0	C	B	A	-	-	MP		< 4700 (1 K code)	-
Clear Page (4) - 16 Bits	CLS	0	1	1	0	0	1	0	1	X	X	0	A*	B*	-	-	-	MP		< 3500 (1 K code)	-
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	-	-	-	-	-	-	-	1	-
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	X	X	0	-	-	-	-	-	-	-	1	-
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	-	-	-	-	-	Y	-	2	-
No Operation	NOP	1	0	0	1	0	0	0	1	0	0	0	-	-	-	-	-	-	-	1	-

9347-18.TBL

s, $\overline{s}$: Source, Destination
01 : Source = MP, Destination = AP
10 : Source = AP, Destination = MP

a, $\overline{a}$: Stop Condition
01 : Stop at End of Buffer
10 : No Stop

r : Indirect Register Number

\- : Not Affected
W : Used as Working Register
X : Set or Reset Buffer
I : Pointer Incrementation
D : Data
MP : Main Pointer
AP : Auxiliary Pointe

(1) Unit : 12 clock periods (≈ 1µs) without possible suspension

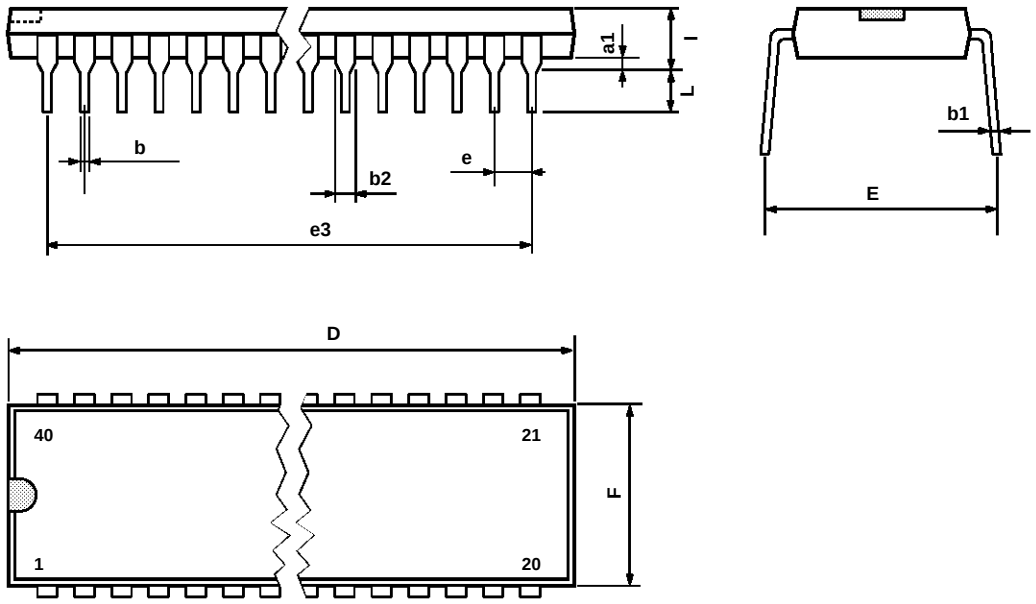
(2) n : Total Number of Words ≤ 40

(3) These commands repeat TLM or KRO with Y incrementation when X overflows. When the last position is reached in a row Y is incremented and the progress starts again on the next row theses command stop only. They can also be used to initialize the page 80 char/row by writing character pairs.

9347-19.TBL

PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL