VQ7254 SERIES

Siliconix incorporated

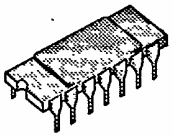
T-43-25

N- and P-Channel Enhancement-Mode MOS Transistor Arrays

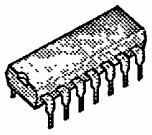
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$	I_D (A)	PACKAGE
VQ7254J	20/–20	3 Ω	2	Plastic
VQ7254P	20/–20	3 Ω	2	Side Braze

14-PIN DIP SIDE BRAZE

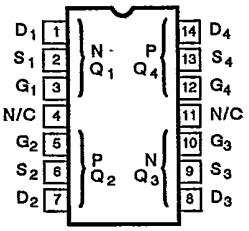


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

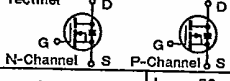
PARAMETERS/TEST CONDITIONS		SYMBOL	VQ7254J		VQ7254P		UNITS
			N-Channel	P-Channel	N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	20	–20	20	–20	V
Gate-Source Voltage		V_{GS}	±30	±30	±20	±20	
Continuous Drain Current (T_A = 25°C)		I_D	2	–2	2	–2	A
Pulsed Drain Current[1]		I_{DM}	±3	±3	±3	±3	
Power Dissipation – Single	T_A = 25°C	P_D	1.75	1.75	1.75	1.75	W
	T_A = 80°C		1.05	1.05	1.05	1.05	
Operating Junction		T_J	–40 to 100				°C
Storage Temperature		T_{stg}	–40 to 150				
Lead Temperature (1/16" from case for 10 seconds)		T_L	300				
Thermal Coupling Factor – Single (K)–Q_1–Q_4 or Q_2–Q_3			60				%
Thermal Coupling Factor – Single (K)–Q_1–Q_2–Q_3–Q_4, Q_1–Q_3 or Q_2–Q_4			50				

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ7254J	VQ7254P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
			VQ7254			
PARAMETER	SYMBOL	TEST CONDITIONS[6]	TYP[2]	MIN	MAX	UNIT
STATIC[4]						
Drain-Source On Voltage	$V_{DS(ON)}$	V_{GS} = 11.4 V, I_D = 1 A ($Q_1 + Q_2$) or ($Q_3 + Q_4$)	2.5	2	3	V
Drain-Source On-Resistance[3]	$r_{DS(ON)}$		2.5	2	3	Ω

			N-Channel			P-Channel			
PARAMETER	SYMBOL	TEST CONDITIONS[6]	TYP[2]	MIN	MAX	TYP[2]	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	-40	20		-55	-20		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8		-3.6	-0.8		
		T_J = 85°C	1.2	0.65		-3.3	-0.65		
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V	±1		±100	±1		±100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.1		500	-0.1		-500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8			-1.6			A
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V, f = 1 MHz	85		175	130		190	pF
Output Capacitance	C_{oss}		80		95	75		100	
Reverse Transfer Capacitance	C_{rss}		18		25	20		60	
SWITCHING[5]									
Turn-On Time	t_{ON}	V_{DD} = 17 V, R_L = 15 Ω, I_D = 1.1 A, V_{GEN} = 10 V, R_G = 25 Ω	12		20	20		30	ns
Turn-Off Time	t_{OFF}		14		20	20		30	
DYNAMIC									
Continuous Source Current (Body Diode)	I_S	Modified MOSPOWER symbol showing the integral P-N junction rectifier 			2			-2	A
Source Current (Body Diode)	I_{SM}				3			-3	
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, T_C = 25°C, I_S = 50 mA	0.6		0.75	-0.6		-0.75	V
		I_S = 1 A	1		1.2	-1		-1.2	

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test: PW = 300 µs, duty cycle ≤ 2%.
4. $r_{DS(ON)}$ and $V_{DS(ON)}$ limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
5. Switching time is essentially independent of operating temperature.
6. Reverse polarity for p-channel devices.

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